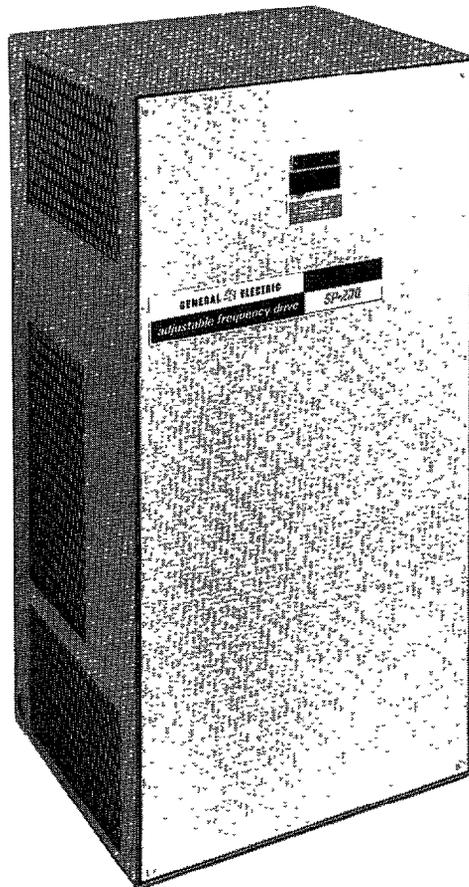


# ST INVERTER ADJUSTABLE-FREQUENCY AC DRIVE

(DRIVE CODE AF-3090)

THEORY OF OPERATION  
FOR 4-, 10-, AND 20-KVA UNITS



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# ST INVERTER ADJUSTABLE FREQUENCY AC DRIVE

NOTE: REFER TO GEK-22958 FOR INSTALLATION, OPERATION, AND TROUBLESHOOTING INSTRUCTIONS.

## THEORY OF OPERATION

A brief description of circuit operation for the basic power unit will be presented in this section. In order to simplify the description, the complete circuit will be divided according to the function performed. A partial elementary diagram for each division will be used to describe that portion of the circuit. The complete circuit is shown on the elementary diagram supplied with the equipment.

It is the purpose of this section to provide a basic understanding of circuit operation which should be helpful in the operation and maintenance of ST-INVERTER drives.

### POWER UNIT BLOCK DIAGRAM

(Figure 1)

The ST-INVERTER power unit will convert 3 $\phi$  AC line power to adjustable voltage DC and invert the DC to adjustable voltage frequency AC power. The simplified block diagram of Figure 1 shows the major circuit sections required to perform this function.

Three phase AC power is converted to adjustable voltage DC by half-wave phase controlled rectifiers. This DC is then converted to adjustable frequency AC by controlled switching of the rectifiers in a 3 $\phi$  inverter bridge. A single speed reference signal is supplied through a timed acceleration and deceleration circuit to both the voltage regulator and frequency control circuits. The voltage regulator controls the DC voltage supplied to the inverter and the frequency control circuit sets the inverter SCR switching sequence, thus controlling the volts per hertz ratio of power supplied to the load. A separate commutation circuit controlled by the frequency control circuit will turn off the inverter SCR's at the proper time.

### START-UP CIRCUIT (Figure 2)

When the start button is pressed relay 2CR will pick up through 18D, 19D, and the normally closed contact of 1CR. Relay 2CR will seal in through contact 2CR3, release the reference voltage set on the speed potentiometer and apply voltage to the control circuit of 1CR

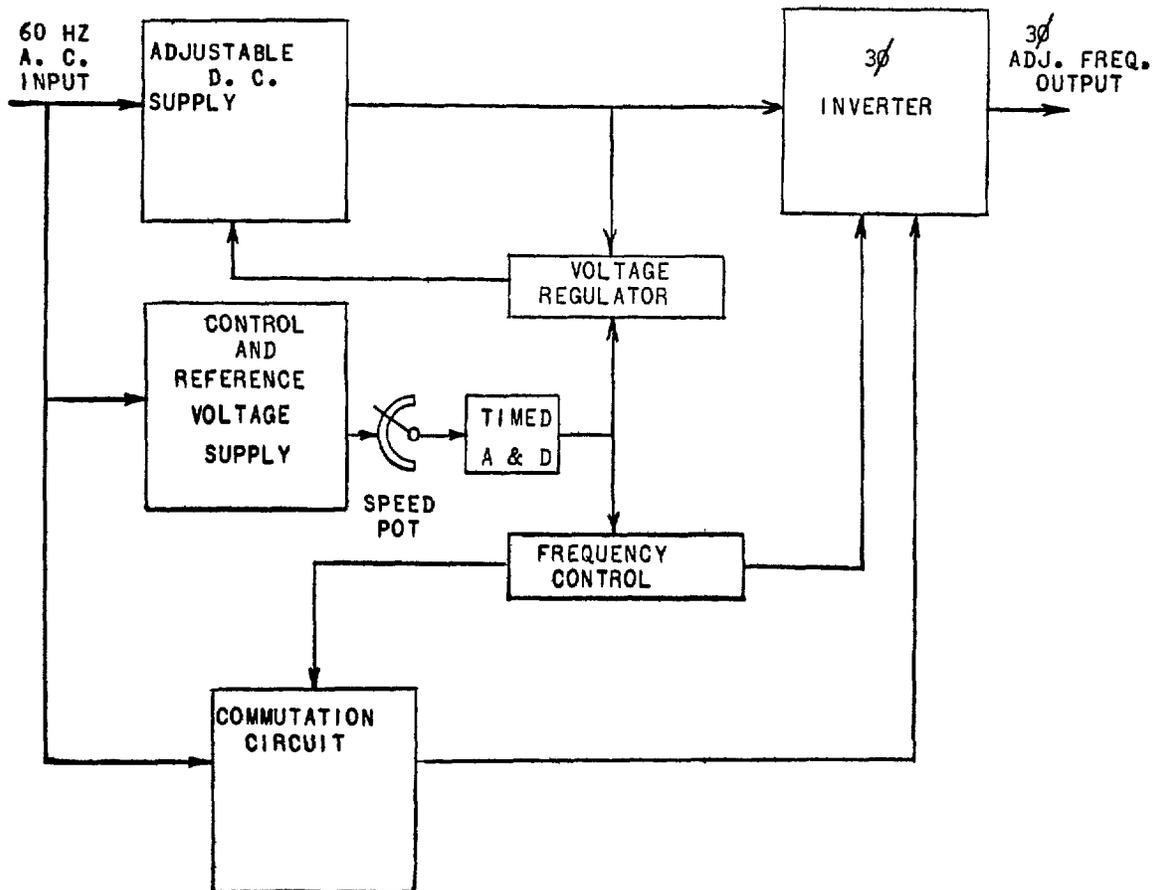


Figure 1. Power Unit Block Diagram

*These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.*



**CONTROL POWER SUPPLIES AND REFERENCE INPUT CIRCUIT (Figure 3)**

Power for the three control voltage power supplies is obtained directly from the input lines through half wave rectifiers 1D, 2D, and 3D. The voltage for the startup relays is zener-regulated at 18.6 volts DC  $\pm$  10% by 3, 4 and 5BD. Voltage-dropping resistor 8R limits the current in the zener diodes and filtering is provided by capacitor 5C. Transistor 2Q regulates the voltage supply for the firing circuits by controlling the current through voltage-dropping resistors 10R, 11R, and 99R. The regulating point of transistor 2Q is set at 44 volts DC  $\pm$  10% by zener diodes 1BD and 2BD. Transistor 1Q operates as a switch to turn 2Q full on, which will essentially short the 44 volt buss to zero. The operation of transistor 1Q is controlled by the I. O. C. trip circuit that is described in another section.

Voltage for the control circuitry is zener-regulated at 24.8 volts DC  $\pm$  10% by 9, 10, 11, and 12BD. The voltage-dropping resistor 9R limits the current in the zener diodes and filtering is provided by capacitor 18C.

The input reference voltage at circuit point 43, which

controls both output frequency and voltage, can be adjusted between 0 and 12 volts by changing the slider position on potentiometer 2P. Resistor 42R forms a divider circuit with 2P so that the reference voltage available across the potentiometer will be approximately 12 volts. The normally closed contact of relay 2CR holds the input voltage at zero, regardless of the setting of potentiometer 2P until relay 2CR is energized by pressing the start button. Diode 25D and resistor 43R provide a fixed diode drop so that the voltage at 44 will be slightly positive when the voltage at 43 is zero. This is necessary to insure that the inverter starts with a minimum delay after the start button is pressed. Diode 100D will limit the reference voltage at 43 to approximately 13 volts.

**TIMED ACCELERATION AND DECELERATION CONTROL CIRCUIT (Figure 4)**

The DC voltage level at circuit point 45 will control both the DC power bus level and the output frequency. This voltage will be the same as the voltage at point 44 which was set by potentiometer 2P. However, the voltage at point 45 will increase and decrease at a linear timed rate determined by the constant current charging and discharging of capacitor 11C through transistors 13Q and 14Q. The current in 13Q and 14Q

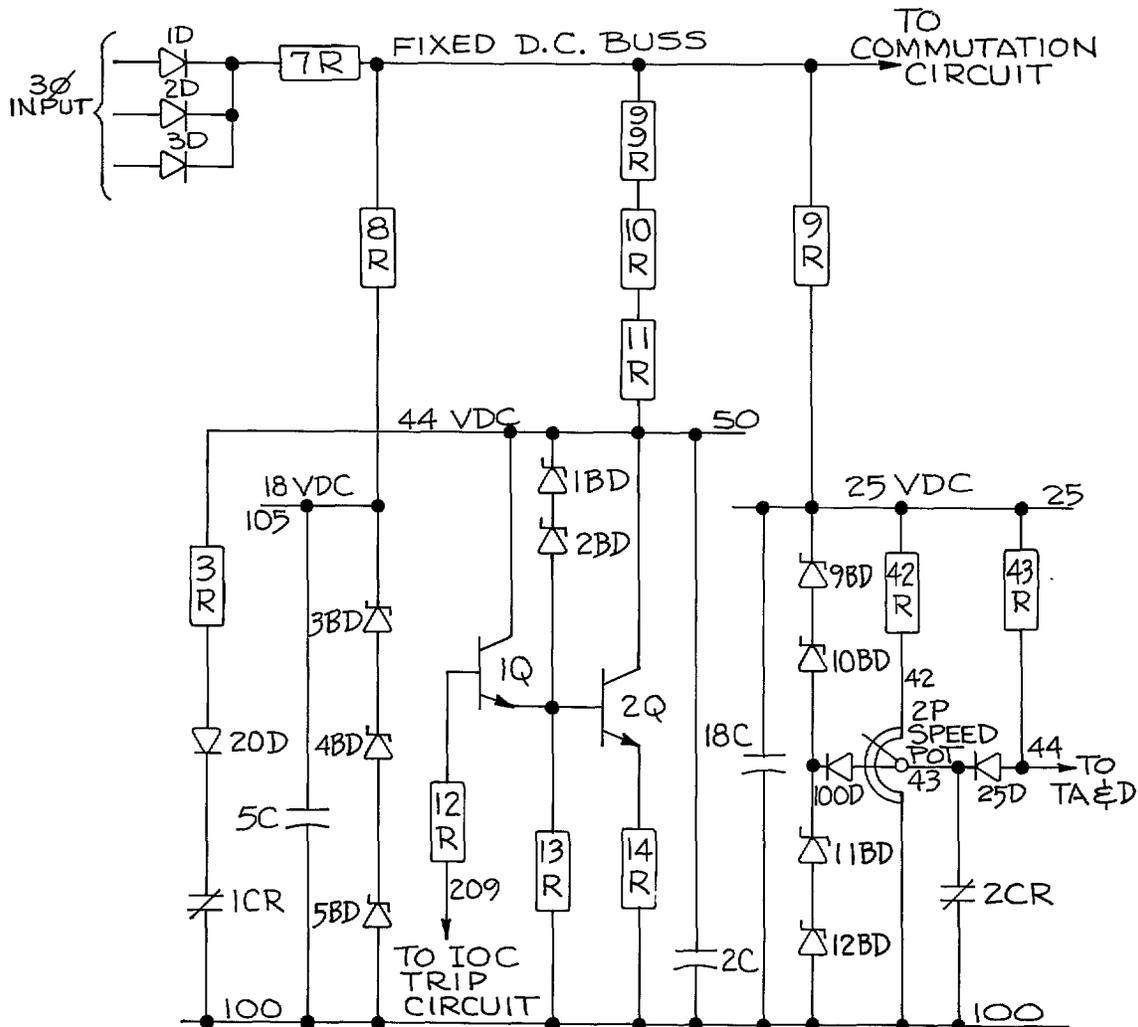


Figure 3. Control Voltage Power Supplies and Reference Input Circuit

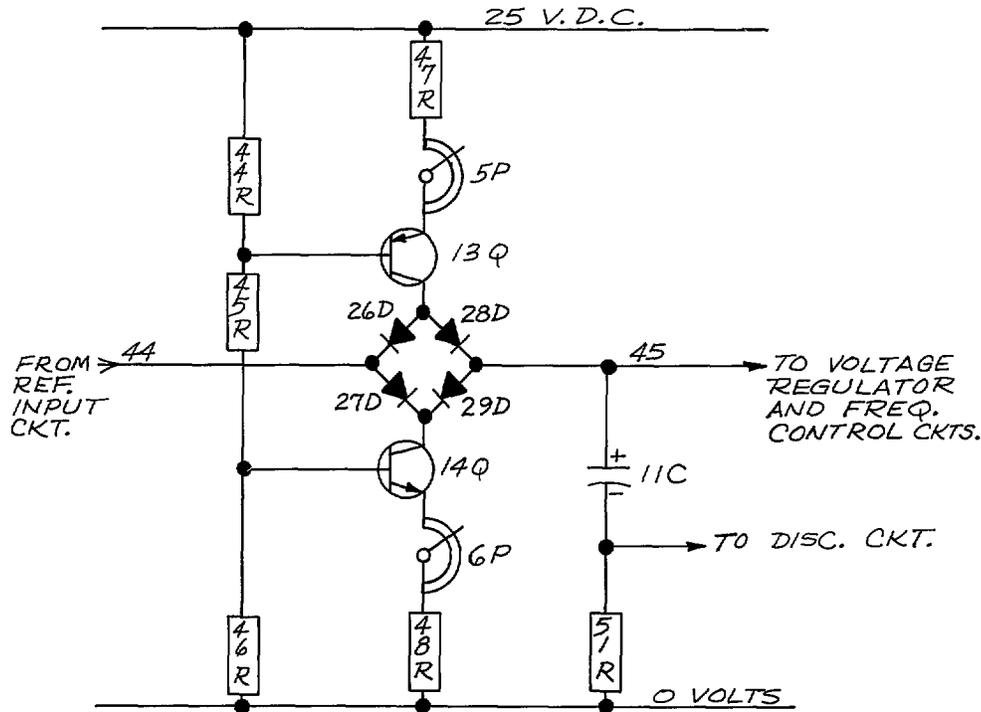


Figure 4. Timed Acceleration and Deceleration Control Circuit

is set by the voltage across divider resistors 44R and 46 R and the value of emitter resistance. These values of resistance are identical and the time will normally be adjusted for approximately 20 seconds. This will be the time required to charge 11C from 0 to 12 volts or discharge from 12 volts to 0, even though the voltage at point 44 may cover this range instantaneously. Other times may be set by adjusting rheostats 5P and 6P. The diode bridge provides decoupling which will allow capacitor 11C to charge through 13Q and 28D or discharge through 29D and 14Q depending on whether the voltage at 44 is higher or lower than the voltage at 45.

#### DC VOLTAGE REGULATOR CIRCUIT (Figure 5)

The reference voltage at point 45 will have the same magnitude as the voltage at point 43 which has been set by potentiometer 2P. Feedback voltage from the DC buss is developed across resistor 54R. The ratio of reference voltage to DC bus voltage is determined by the ratio of 54R to the total resistance of 2R, 49R 1P, 124R, and 54R. This ratio is normally set by adjusting 1P so that 12 volts on the base of 15Q will correspond to 128 volts on the DC buss. The current in transistor 15Q will be proportional to the difference in feedback and reference voltage. This current signal is proportional to the error voltage and will be supplied to the phase control circuits through an emitter follower circuit consisting of transistor 16Q and resistors 52R, 53R, and 55R. Stabilizing is provided by resistor 50R, capacitor 10C, and resistor 52R. Diode 30D and the divider consisting of resistors 126R and 127R is provided to decrease the re-

sponse time of the regulator when fast deceleration is required.

A means for adjusting the voltage boost at low frequency, which is normally required with most AC motors, is provided by the circuit consisting of 123R, 3P, 53Q, and 125R. Adjusting 3P clockwise will cause transistor 53Q to conduct diverting a small portion of the feedback current from the normal path causing the DC buss voltage to increase. This adjustment is effective mainly at the low frequency end of the constant volts per hertz curve.

The operation of only one phase control circuit will be covered since these are identical for each of the controlled rectifiers (1SCR, 2SCR, and 3SCR) in the 3Ø input circuit. Transistor 17Q will turn the gating pulses supplied to 1SCR off and on at the proper time during each positive half cycle of the line 1 to neutral voltage. These gating pulses are generated in the firing circuit which will be described later. When transistor 17Q turns on, gating pulses will also be turned on. Thus, the point at which 1SCR turns on during each positive half cycle of line to neutral voltage is directly related to the operation of 17Q.

In order to synchronize the operation of 17Q with the line 1 to neutral voltage and provide smooth phase control, a portion of this voltage is shifted approximately 95° leading and supplied to the base. The RC circuit consisting of resistor A and capacitor 12C shifts the voltage 90° and the additional 5° shift is provided by resistor B and 13C.

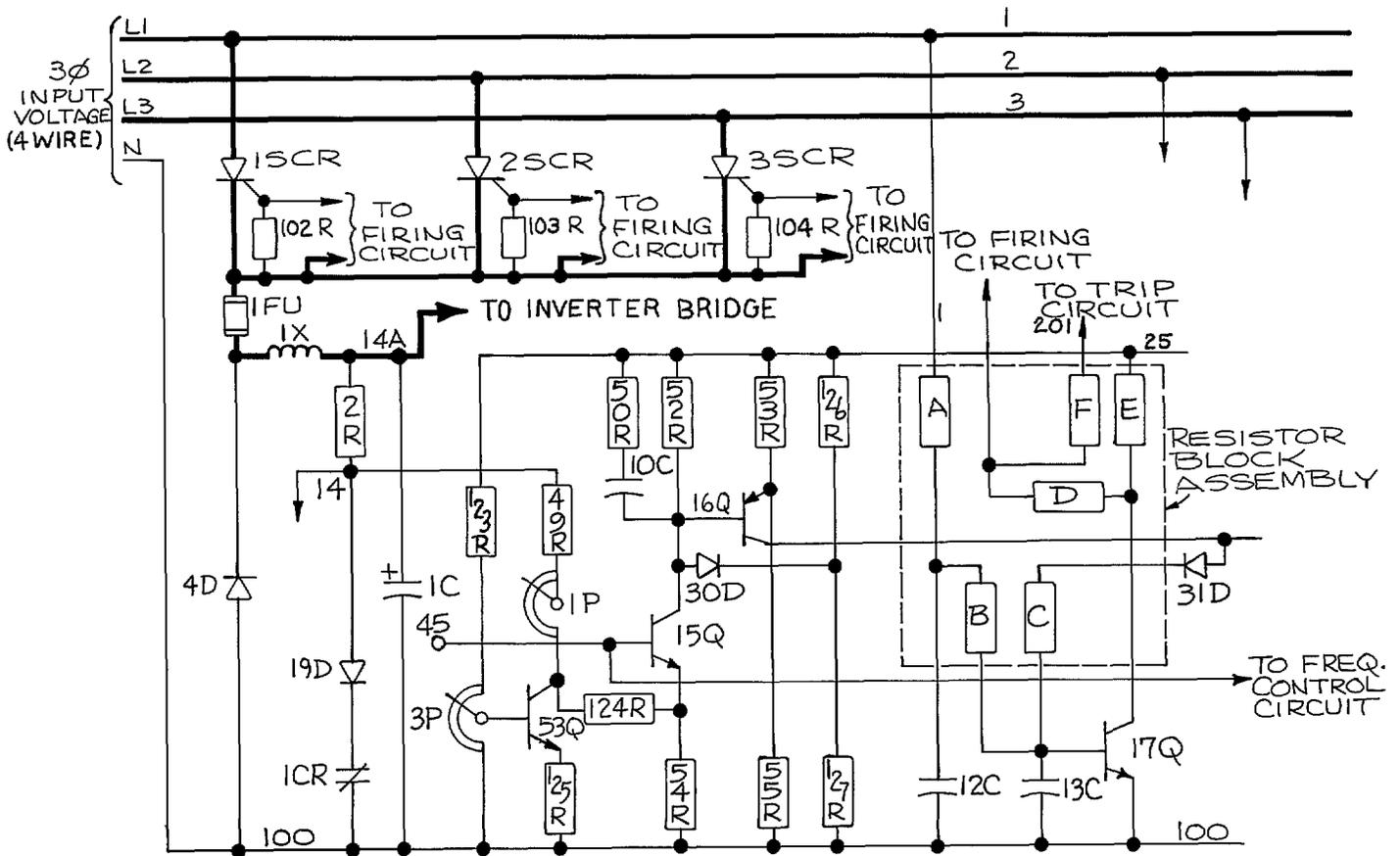


Figure 5. DC Voltage Regulator Circuit

The point that 17Q turns on during the half cycle is determined by the amount of current supplied to the base from the voltage regulator circuit. For example, if the reference voltage at point 45 is increased, there will be a proportional increase in current through 15Q and 16Q resulting in more current being supplied to the base of 17Q through 31D and resistor C. This increase in current will cause the transistor and 1SCR to turn on earlier in the half cycle increasing the DC buss voltage; A decrease in feedback voltage would have the same effect. Of course a decrease in reference voltage or an increase in feedback voltage would have the opposite effect. A signal from the IOC trip circuit through resistor F will bypass the phase control circuit and turn off the gating pulses to 1SCR.

The three SCR's will control the current supplied to 1C during each positive half cycle of the line 1, 2, and 3 to neutral voltage. Reactor 1X limits the peak current in the capacitor and diode 4D will prevent the SCR cathode voltage from going negative at the low end of the adjustable voltage range and reduce the ripple.

Fuse 1FU will protect the input SCR's in the event of a short circuit in the DC circuit. This fuse will not

protect the inverter bridge SCR's. The normally closed contact of 1CR will discharge capacitor 1C through 2R and 19D.

#### FREQUENCY CONTROL CIRCUIT (Figure 6)

Frequency control for the inverter portion of the circuit is provided by the oscillator consisting of 2FL, 57R, 19C, 20Q, 4P, 58R, and 2X. The operation of this oscillator is as follows. Capacitor 19C will charge through 20Q, 4D and 58R until the breakover voltage of 2FL is reached. At this point 2FL will change from the blocking state to a very low impedance conducting state discharging 19C through 57R and 2X. When 19C has discharged, the current in 2X will continue to flow, momentarily reversing the voltage on 19C which causes 2FL to revert back to the blocking state, and the cycle repeats. Each time 2FL conducts, transistor 21Q will turn on causing the voltage at point 80 to drop. The negative going pulses produced at this point are supplied to the ring counter which will be discussed later.

The rate at which pulses occur depends upon the charging current for 19C which is controlled by 20Q. This current is governed by the voltage signal delivered to

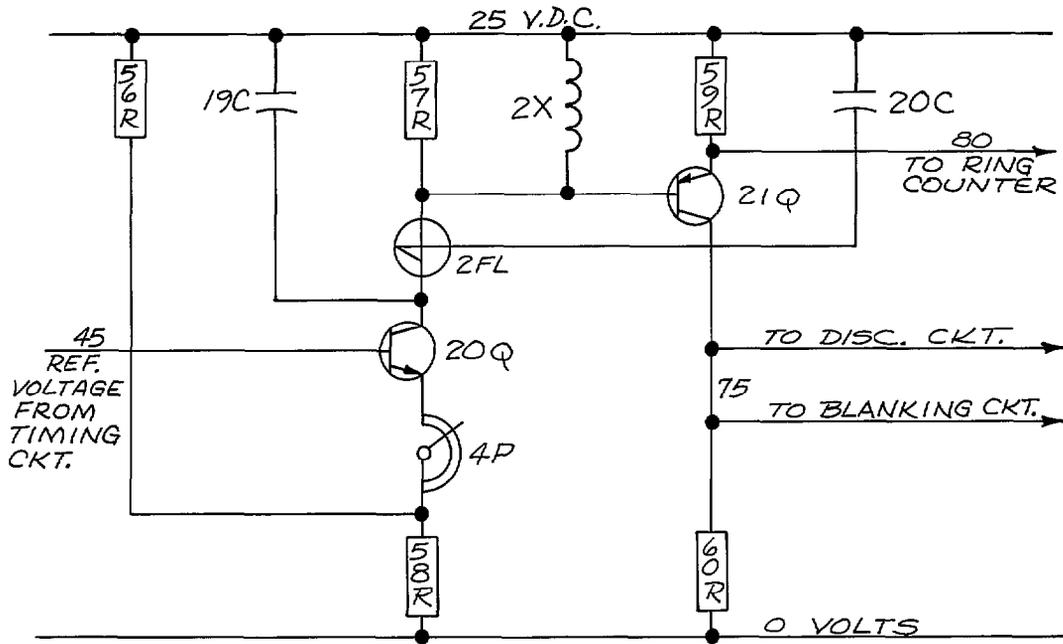


Figure 6. Frequency Control Circuit

the base of the darlington amplifier 20Q which converts this voltage signal into a proportional current. The 20Q base voltage signal is in turn obtained from the same basic reference voltage which establishes the level of the DC voltage buss. The charging current for 19C is therefore directly proportional to the DC buss voltage. This provides a constant ratio of volts to frequency as the reference voltage is increased and decreased. Such a constant "volts per hertz" ratio is required in the operation of AC motors.

Rheostat 4P provides a means of adjusting the volts per cycle ratio to match the motor design.

FIRING CIRCUIT (Figure 7)

The firing circuits used on ST-100 drives produce a train of steep wave front high energy pulses suitable for firing conventional and inverter type SCR's. Circuit operation will be as follows:

When power is initially applied, current flows from the 47 volt bus through FC2R into the base of transistor FC2Q, thereby causing FC2Q to conduct and to apply voltage to the primary winding of transformer FC1T. Voltage appearing at secondary winding S1 is positive at terminal 3 with respect to terminal 4. This

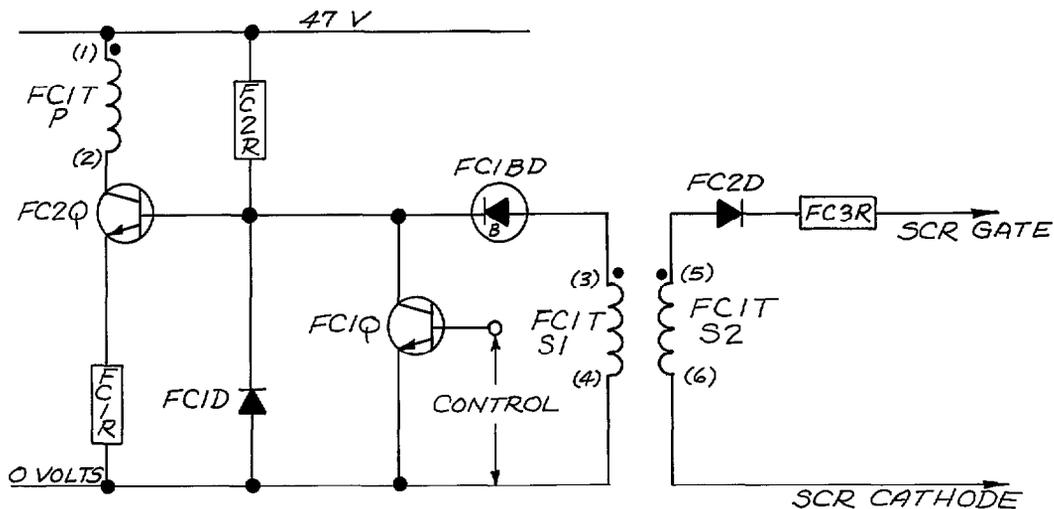


Figure 7. Firing Circuit

voltage will cause more base current to flow in FC2Q turning it fully on. It can be seen that the connection of secondary winding S1 of FC1T in the circuit is regenerative and causes FC2Q to switch on.

The voltage applied to the primary winding will be the supply voltage minus the voltage across resistor FC1R and the saturated transistor voltage. The voltage across FC1R is caused by the flow of transformer load current and exciting current. With time the voltage across FC1R will increase as exciting current increases. Thus, the voltage across the primary winding will decrease, causing a proportional decrease in the voltage developed across secondary S1. Both of these actions are in the direction to eventually cause FC2Q to turn off.

Once transistor FC2Q starts to turn off, the process is regenerative in that direction also. Because of exciting current flowing in the primary winding at the time of turn off, the voltages on all windings will reverse in an attempt to find a path for the ampere turns flowing in the primary. The path is provided by FC1D and FC1BD. The energy trapped in the exciting impedance is eventually delivered at constant voltage (the voltage of zener diode FC1BD) to FC1D and FC1BD. During this time the voltages on all transformer windings are maintained at predetermined values. Also during this time the starting current supplied through FC2R is diverted from the base of FC2Q, thereby providing additional assurance that FC2Q is completely turned off.

After all of the exciting energy has been dissipated, the voltages across all windings go to zero. As a result, the starting current begins to flow through FC2R, into the base of FC2Q and the process starts all over again.

Control of the oscillator is obtained by turning transistor FC1Q on or off. It can be seen that by turning FC1Q on, the feedback path from secondary S1 is shorted out and oscillations will stop even if supply voltage is still present. When transistor FC1Q is turned off, oscillation will start again immediately.

Secondary winding S2 supplies voltage through FC2D, and FC3R to the gate of the SCR. Diode FC2D also prevents the gate to cathode of the SCR from being reverse biased when the voltage on winding S2 reverses.

**BLANKING CIRCUIT (Figure 8)**

The firing pulses supplied to the gates of the six SCR's in the output bridge, will be blanked out for a short period of time following each pulse of the frequency control oscillator. The purpose of this blanking period will be explained in the discussion of operation of the commutation circuit.

Operation of the blanking circuit is initiated by a voltage pulse from the oscillator at point 75 and supplied to the base of 22Q through 61R, 34D and 62R. Prior to a pulse from the oscillator, 23Q will be biased on by current through resistor 64R. When voltage is supplied to the base of 22Q, it will turn on, thus turning 23Q off. The time period, after each pulse from the oscillator that 22Q remains on and 23Q is held off, will be determined by the values of 21C, 62R and 63R. This time will be approximately 90 microseconds. While 23Q is off, current will be supplied to the firing circuit control transistors turning off the firing pulses to all SCR's in the output bridge. This current is supplied from the control voltage buss through 65R and the resistors connected to the firing circuit control point.

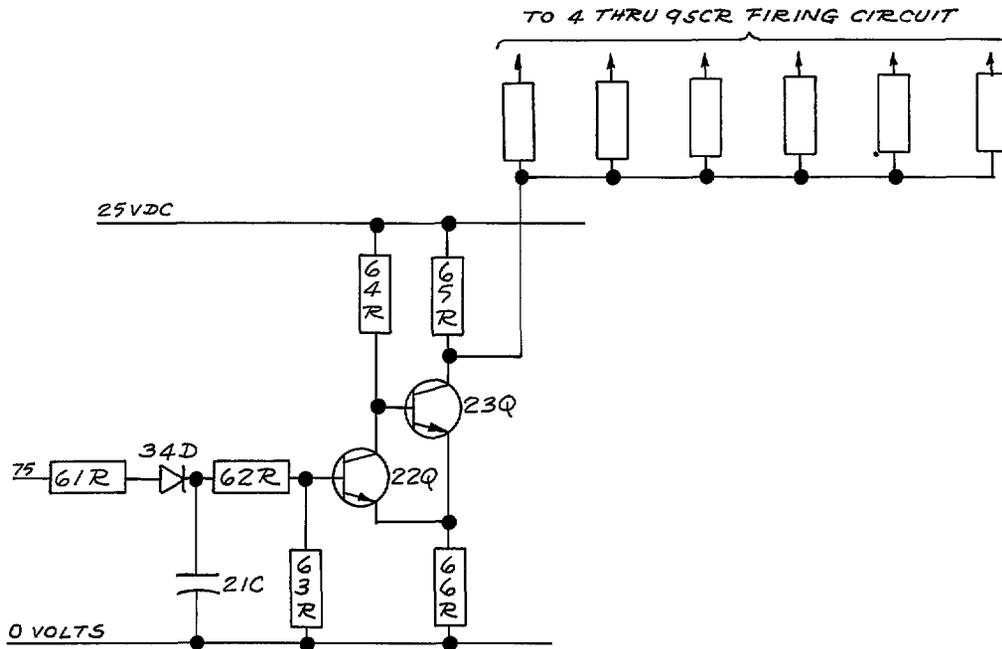


Figure 8. Blanking Circuit

GATING CIRCUIT FOR COMMUTATION SCR'S  
(Figure 9)

This circuit will supply turn-on pulses alternately at 60° intervals, to commutating SCR's 10SCR and 11SCR. It is necessary to coordinate the firing of the commutating SCR's with the gating signals supplied to the inverter bridge SCR's. This coordination is provided by the ring counter circuit.

You will note that capacitors 22C and 24C are each connected through a diode and resistor to the collectors of three transistors in the ring counter. The relationships between ring counter collectors and gating pulses at points 31 and 32 are shown graphically in Figure 10. It can be seen that there will always be one of two conducting collectors in each group. Also, in each group the number of conducting collectors will alternate at 60° intervals between one conducting and two conducting. In addition, when the number of conducting collectors goes from one to two in the first group, the second group will go from two to one.

Normally 24Q and 27Q are conducting and 25Q and 26Q are non-conducting. When the group of ring counter transistors connected to 22C change from one conducting to two conducting, point 89 will receive a negative increment of voltage. This will cause 24Q to turn off and 25Q to turn on delivering a pulse to the gate of 11SCR. The pulse width is limited by means of the current through RB which quickly restores the voltage of the right hand side of 22C to its original, slight-

ly positive, level, turning 24Q on and 25Q off. The next 60° transition point will cause 26Q to deliver a pulse to the gate of 10SCR. These gating pulses will alternate between the two commutating SCR's every 60° as shown in Figure 10. When the current trip circuit operates circuit point 87 goes positive, turning on transistor 52Q. This will pull the collector voltage of 25Q and 26Q down near zero, cutting off the firing pulses to the commutation SCR's.

RING COUNTER CIRCUIT  
(Figure 11)

The ring counter consists of three triggered flip-flops steered from one to another in such a way that successive trigger pulses at circuit point 80 causes the counter to advance from one condition to the next. Steering is such that only six of the eight possible combinations of the flip-flops are used. When each trigger pulse is received, only one of the flip-flops changes state and changes the steering such that when the next pulse is received, another of the flip-flops will change state. Receipt of six pulses brings the counter back to its starting condition. Trigger pulses arrive every 60° of the desired inverter operating frequency. Components 48D, 49D, 50D, 75R, and 76R are used to prevent the counter from starting in either of the two unwanted combinations. The following table shows the sequence of operation of the six collectors in which a logic 0 designation is applied to a conducting transistor and a logic 1 is applied to a non-conducting transistor. This same relationship is shown graphically in Figure 10.

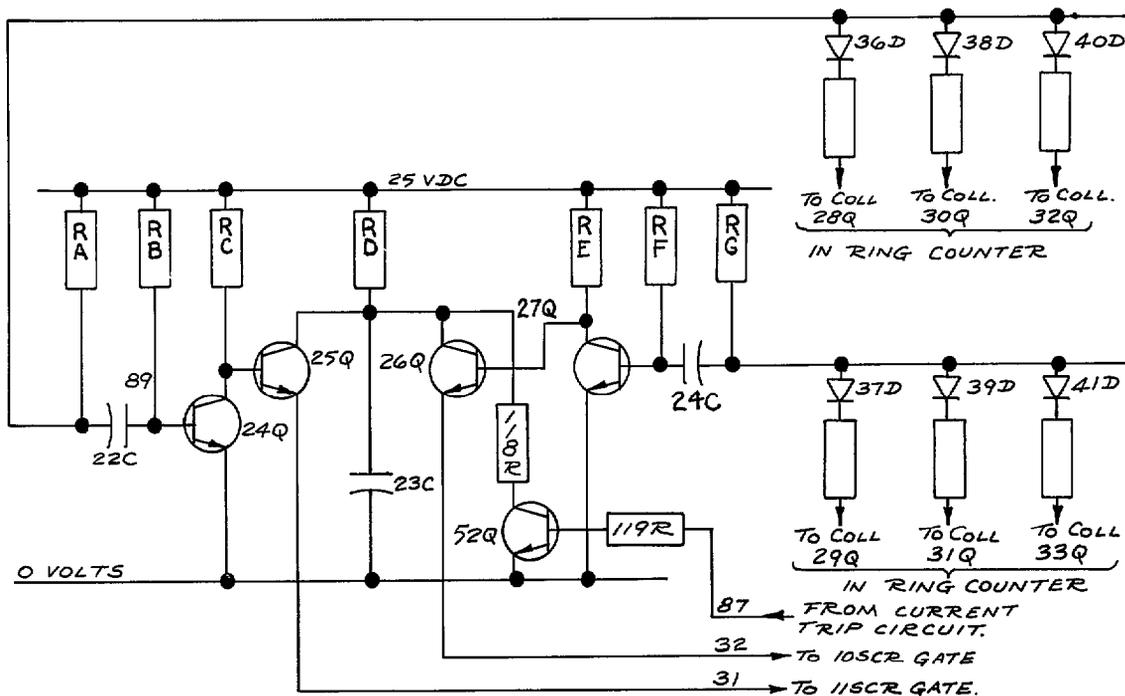


Figure 9. Gating Circuit for Commutation SCR's

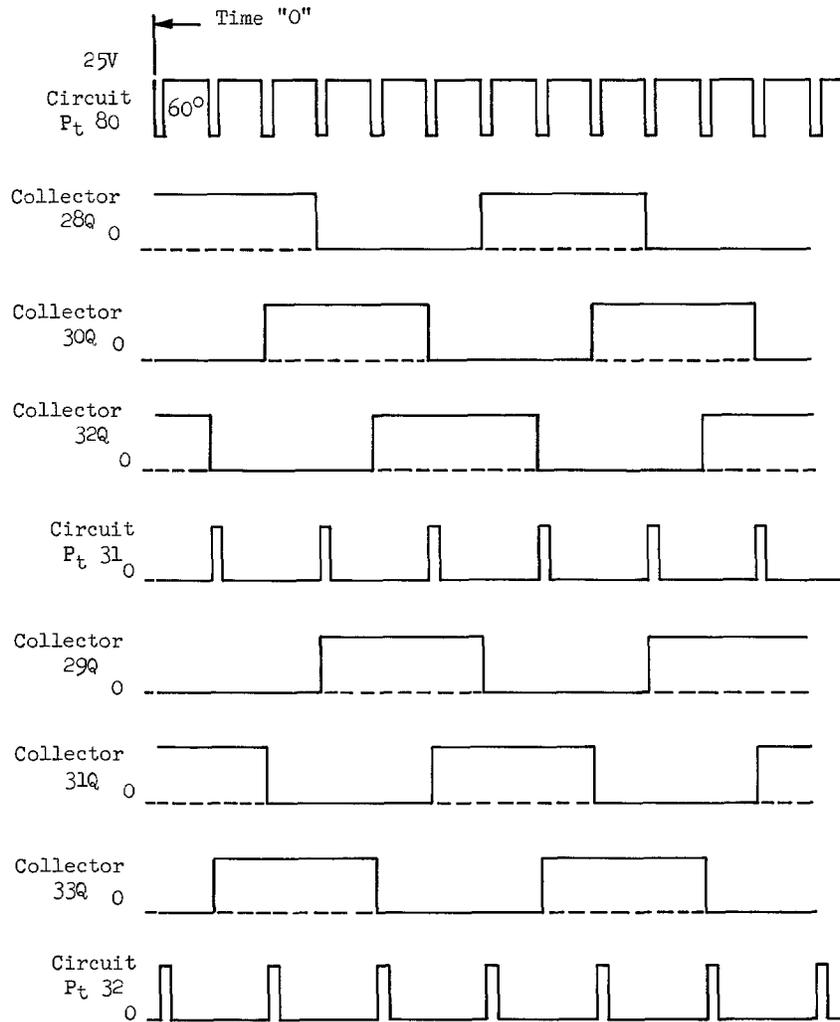


Figure 10. Voltage-Time Relationships

TABLE 1

	TIME	28Q	29Q	30Q	31Q	32Q	33Q
START	0	1	0	1	0	1	0
	60°	1	0	1	0	0	1
	120°	1	0	0	1	0	1
	180°	0	1	0	1	0	1
	240°	0	1	0	1	1	0
	300°	0	1	1	0	1	0
REPEAT	360°	1	0	1	0	1	0

The collectors of the ring counter transistors control the gating signals to the inverter SCR's. Each transistor collector controls one of the SCR's such that when the transistor is conducting, it permits the blocking oscillator firing circuit to supply gating pulses to the SCR it controls.

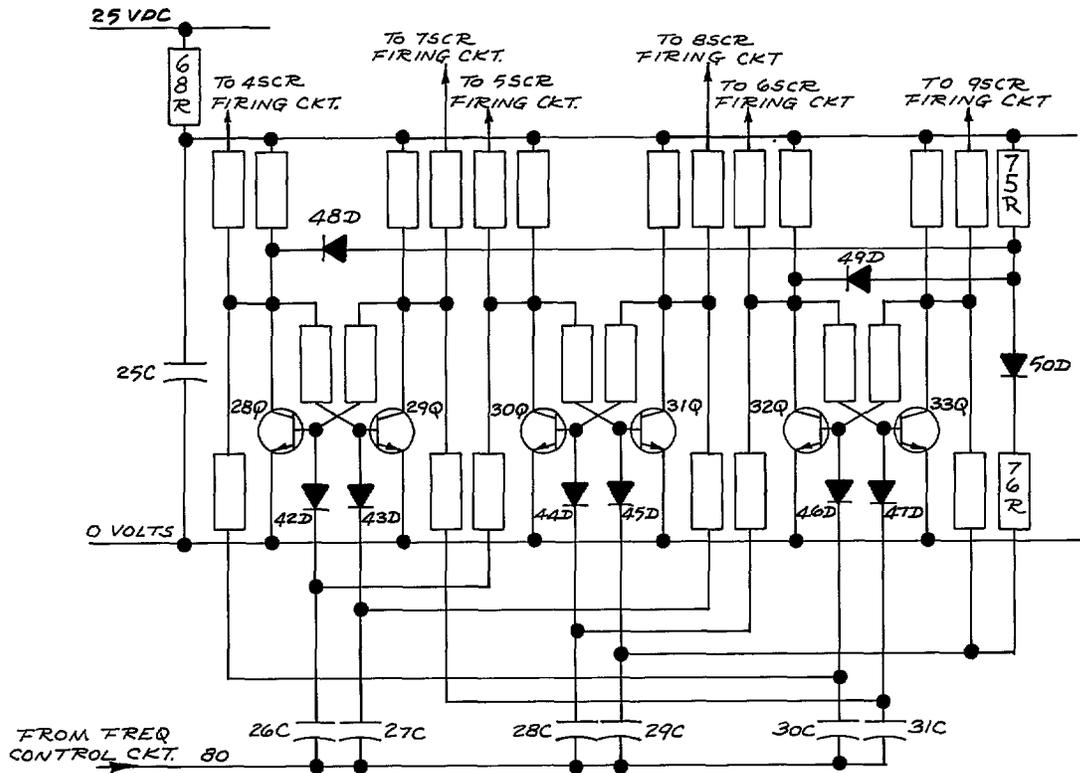


Figure 11. Ring Counter Circuit

**INVERTER BRIDGE** (Figure 12)

The output power circuit consisting of SCR's 4SCR, 5SCR, 6SCR, 7SCR, 8SCR and 9SCR, diodes 8D, 9D, 10D, 11D, 12D, and 13D, and secondary windings of commutating transformers 2T and 3T is a three phase inverter bridge operating from an adjustable DC volt-

age. Power diodes 8D through 13D are connected in inverse parallel with each SCR and make it possible for the inverter to supply lagging loads by providing paths for reverse current flow. Each of the bridge SCR's is operated in synchronism and in phase with its controlling transistor in the ring counter circuit. The following table shows the sequence of transistor operation in the ring counter circuit.

TABLE 2

TIME	4SCR	5SCR	6SCR	7SCR	8SCR	9SCR	TOP ROW	BOTTOM ROW
0	OFF	ON	OFF	ON	OFF	ON	1	2
60°	OFF	ON	ON	ON	OFF	OFF	2	1
120°	OFF	OFF	ON	ON	ON	OFF	1	2
180°	ON	OFF	ON	OFF	ON	OFF	2	1
240°	ON	OFF	OFF	OFF	ON	ON	1	2
300°	ON	ON	OFF	OFF	OFF	ON	2	1
360°	OFF	ON	OFF	ON	OFF	ON	1	2

Also shown in Table 2 is the number of SCR's that are conducting at any one time in the top and bottom rows of SCR's. It will be noted that the total number of SCR's conducting at any one time is three and that these SCR's are always so distributed that there are two conducting in one row and one conducting in the other row. The "two-on" condition alternates be-

tween the bottom and top rows at successive switching points.

In addition, at each switching point, only one SCR is required to change from conducting to non-conducting and only one from non-conducting to conducting. Also, the SCR that goes from conducting to non-conducting

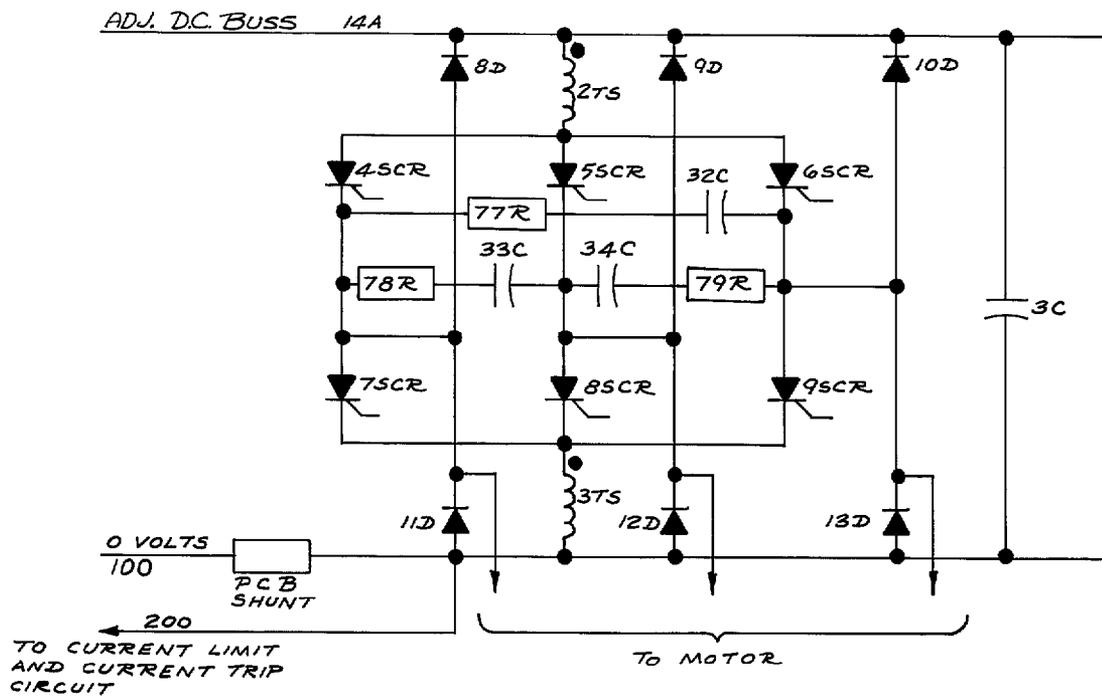


Figure 12. Inverter Bridge

is always one of the two in the same row that have been conducting. Therefore, it is not necessary to turn off all SCR's that are conducting in order to be sure to turn off the one that is actually required to turn off.

It will be necessary to turn off only that row in which two SCR's happen to be conducting. This is accomplished by applying a commutation pulse to only one row of SCR's at one switching point and to the other row of SCR's at the next switching point and so on. These pulses are coordinated with the gating sequence of the SCR's by the ring counter.

The output line to line voltage will be a "quasi-square" wave having a voltage-time relationship as shown in Figure 13. Such a wave has no harmonic voltage below the fifth. The RMS fundamental component (superimposed) will be 0.78 times the peak which is deter-

mined by the adjustable DC voltage supplied to the inverter.

#### COMMUTATION CIRCUIT (Figure 14)

Diodes 1D, 2D, and 3D supply current directly from the line through current limiting resistor 7R to charge capacitor 35C. The voltage across 35C will have a magnitude nearly equal to the peak of the input AC voltage. This provides a fixed DC voltage to supply the commutating circuit which consists of 4T, 36C, 2T, 3T, 15D, 10SCR and 11SCR. During a typical commutation cycle current will flow through reactor 4T and diode 14D to charge capacitor 36C. With no charge on 36C at the beginning of the charge cycle, the full 150 volts will initially appear across reactor 4T. When capacitor 36C is charged up to 150 volts, the energy stored in reactor 4T will keep the current flowing until the capacitor is charged to approximately

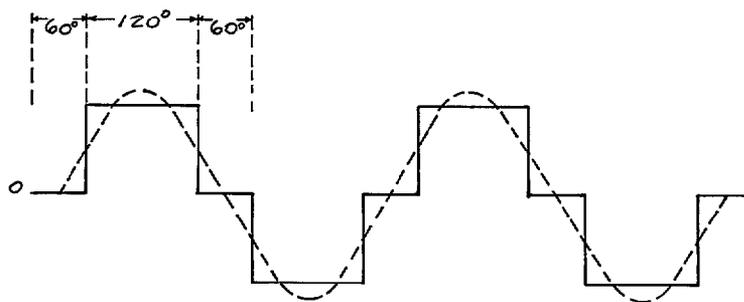


Figure 13. Inverter Output Line to Line Voltage

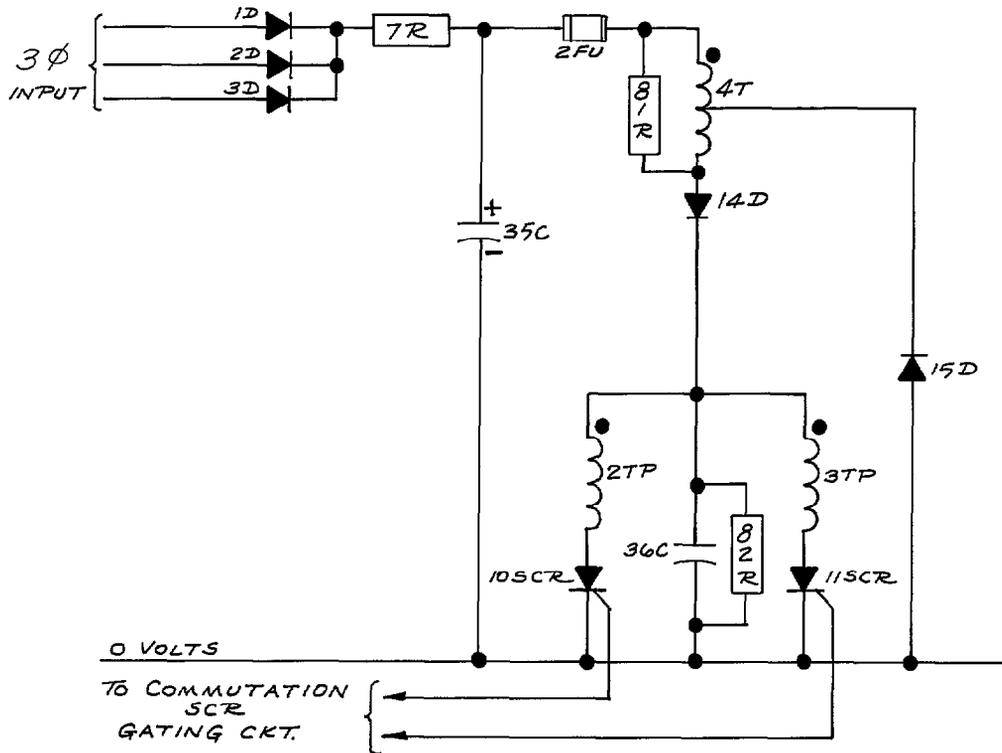


Figure 14. Commutation Circuit

300 volts. Diode 14D prevents the capacitor from discharging back through the reactor.

Capacitor 36C will be discharged through either transformer 2TP and 10SCR or transformer 3TP and 11SCR. You will note in the inverter bridge circuit that the secondary winding of 2TS connects the top row of SCR's to the top buss and 3TS connects the bottom row of SCR's to the bottom buss. Gating on 10SCR will cause a positive voltage to appear at the dotted ends of the primary and secondary windings of transformer 2T and a negative voltage at the undotted ends. This voltage on winding 2TS will put a reverse voltage on the top row of SCR's. The magnitude of reverse voltage will be 300 volts minus the adjustable DC bus voltage.

When 11SCR is gated on, the same magnitude of reverse voltage will appear across the bottom row of SCR's. The required sequence for gating on commutation SCR's is given in the description of the inverter bridge circuit.

When commutation is initiated, the load current flowing in secondary winding 2TS is transferred to primary winding 2TP. This initial current in 2TP is replaced by the flow of discharge current from capacitor 36C. As the voltage across 36C decreases, the voltages across windings 2TP and 2TS decrease accordingly. At some point the anode to cathode voltage on the top row of SCR's will become positive again. If gating is withheld from these SCR's at this time, they will not conduct and current will not flow in winding 2TS.

When the voltage across capacitor 36C reaches zero, the voltage across winding 2TP will reverse and charge 36C in the negative direction. This reverse charge on capacitor 36C turns off 10SCR.

Diode 15D limits the negative voltage on 36C to the voltage level at the top of reactor 4T and pumps the excess energy back into the supply. For diode 15D to be effective in returning energy to the supply, it is necessary to prevent the top row of SCR's from being gated on immediately after commutation. This function is provided by the blanking circuit.

When the energy in winding 2TP is exhausted, the current will go to zero and the recharge cycle starts over again. Gating on 11SCR will initiate the next commutation cycle.

#### CURRENT LIMIT CIRCUIT (Figure 15)

The current limit circuit will operate to reduce the output voltage and frequency when the DC current to the inverter bridge exceeds a preset level. This level, which is the current limit point, is fixed at approximately 150% of the power unit continuous rating.

A voltage signal proportional to current in the DC power circuit is developed across a calibrated shunt. This small voltage signal is amplified by the circuit consisting of transistors 9Q and 10Q and resistors 32R, 33R, 34R, and 100R. Transistor 11Q is connected to operate as a diode and with the current flowing through resistor 35R provides a bias voltage

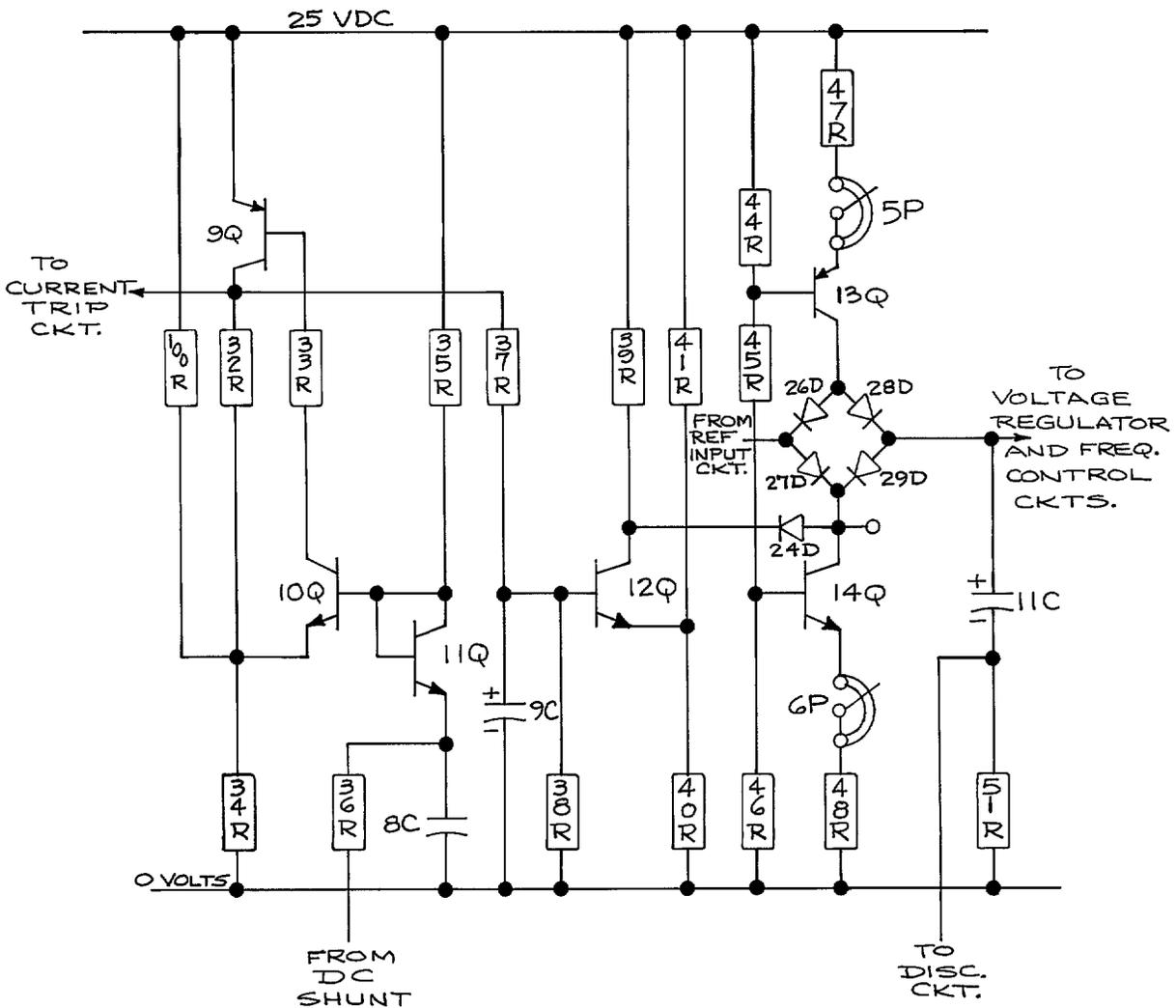


Figure 15. Current Limit Circuit

that will closely match the base to emitter drop of transistor 10Q. An additional bias voltage on the emitter of 10Q from the voltage divider consisting of 100R and 34R will insure that the amplified voltage at the collector of 9Q tracks the signal voltage starting at zero.

The signal voltage from the shunt will appear across capacitor 8C and cause the base voltage of 10Q to raise by the same amount. This will cause transistor 10Q to conduct providing base drive for transistor 9Q. The resulting current flow from 9Q through resistors 32R and 34R will cause the emitter voltage of 10Q to equal the signal voltage on the base.

The amplifier output voltage at the collector of 9Q is equal to the voltage drop across both resistors 32R and 34R. It can be seen that the amplification of the signal voltage will be equal to the ratio of 32R to 34R plus one. For example, the typical average signal voltage from the shunt to initiate current limit

on 10 KVA inverters will be approximately 0.6 volt and the value of 32R and 34R is 22K and 1.5K. This means that the signal voltage will be amplified by a factor of approximately 15 resulting in an output voltage of 9 volts.

The signal voltage from the shunt has a sawtooth wave-shape and a frequency that is 6 times the inverter output frequency. The average value of a portion of the amplified signal voltage will appear across capacitor 11C on the base of transistor 12Q. When the base voltage of 12Q exceeds the bias voltage on the emitter, determined by the value of resistors 41R and 40R, transistor 12Q will start to conduct. This will draw current from the timing circuit through diodes 24D and 29D causing the voltage across capacitor 11C and resistor 51R to decrease. The inverter output voltage and frequency will also decrease since the voltage across 11C and 51R is the reference voltage for the voltage regulator and frequency control circuits. The output voltage and frequency will continue

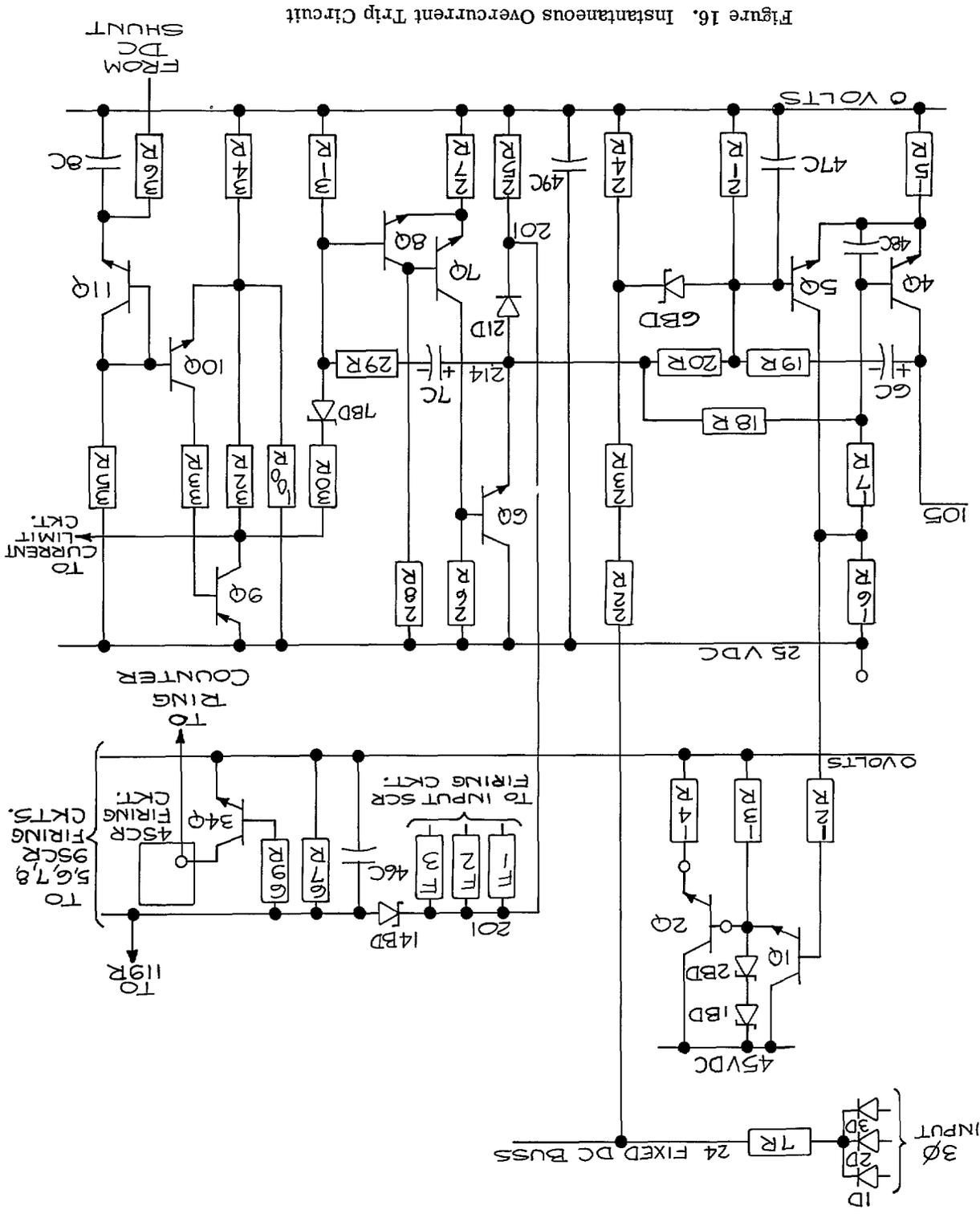


Figure 16. Instantaneous Overcurrent Trip Circuit

The IOC circuit will shut down the inverter power unit and protect the bridge SCR's when the peak current in the DC power circuit exceeds a preset level. This level, which is the trip point, will normally be set

(Figure 16) INSTANTANEOUS OVERCURRENT TRIP CIRCUIT

1. Turn the input SCR's off.
  2. Turn all bridge SCR's on.
  3. Drop out the start relays 1CR and 2CR.
  4. Remove firing pulses from the commutation SCR's.
- When the trip point is exceeded the IOC circuit will perform the following functions instantly.

slightly below the commutation capability of the inverter.

to decrease as long as the load increases.

The DC power buss capacitor 1C (see Figure 5) immediately discharges through the bridge SCR's and the inverter shuts down. Since the discharge current of capacitor 1C is shared by the SCR's in the three legs of the bridge they will not be damaged. Without the IOC circuit the discharge current of capacitor 1C would probably be carried by only one leg of the bridge resulting in SCR damage. Since the operation of the IOC circuit is instantaneous the bridge SCR's will be protected from damage that would normally result from a commutation failure or line to line short on the output.

The IOC circuit will operate when the peak current in the calibrated shunt results in a voltage at the collector of 9Q that exceeds the breakover voltage of zener diode, 7BD. (Operation of the DC amplifier circuit 9Q and 10Q is described in the current limit section.) Normally 8Q is off and 7Q is held on by current through resistor 28R causing 6Q to remain off. When current flows through 30R and 7BD transistor 8Q will turn on. This will cause 7Q to turn off and 6Q to turn on. The voltage at circuit points 214 and 201 will immediately increase to a level near the 25 volt buss voltage. The voltage at 201 will cause current flow through resistors F1, F2, and F3 turning off the firing circuits that supply gating to the input SCR's, 1SCR, 2SCR and 3SCR. This voltage will also cause current to flow through zener 14BD supplying base current to transistor 34Q through resistor 69R. Transistor 34Q will turn on forcing the firing circuit to supply gate pulses continuously to 4SCR in the inverter bridge. This operation is duplicated at each of the remaining five firing circuits (by transistors 35Q to 39Q) that supply gating to the bridge SCR's. Voltage is also supplied to resistor 119R and transistor 52Q (see Figure 9) in the commutation SCR firing circuit turning off the gate pulses to 10SCR and 11SCR.

The conditions described above will remain as long as 6Q is conducting.

As stated earlier, the start relays 1CR and 2CR will also drop out when the IOC circuit operates. This is accomplished by turning on transistor 4Q which pulls the relay supply voltage down to near zero, causing the relays to drop out. Transistor 4Q is

turned on by base current supplied from point 214 through resistor 18R.

When the IOC circuit operates the voltage at 214 will cause capacitor 7C to charge with polarity shown through resistor 29R. This charging current will hold transistor 8Q on which also holds 6Q on for a fixed period of time to insure that all functions of the IOC circuit are completed.

After the IOC circuit operates the inverter will remain off until the start button is pressed.

#### UNDER VOLTAGE TRIP CIRCUIT (Figure 17)

The under voltage trip circuit will safely shut down the inverter power unit when the input line voltage is momentarily lost or drops below approximately 80% of normal. Operation of the under voltage circuit is initiated by a drop in the fixed DC buss level which is supplied directly from the input line voltage.

The divider network consisting of 22R, 23R and 24R provides a portion of the DC buss voltage across 24R. This voltage will normally exceed the zener voltage of 6BD and hold transistor 5Q on. When transistor 5Q is on transistors 4Q and 1Q will be off.

If the fixed DC buss level drops to a point where the voltage across 24R is below the zener voltage of 6BD transistor 5Q will turn off. When 5Q turns off current will flow through 16R and 17R into the base of 4Q and through 12R into the base of 1Q turning both transistors on. The conduction of transistor 1Q will cause 2Q to turn full on essentially shorting the 45 volt buss. Since this buss supplies all firing circuits, gating pulses will be removed from both the input and bridge SCR's. Transistor 4Q will short the relay supply buss 105 causing relays 1CR and 2CR to drop out which immediately shuts down the power unit.

Although the drop in voltage across resistor 24R may be momentary, the normal voltage polarity on capacitor 6C, as shown, will hold transistor 5Q off for a sufficient length of time to insure that the above functions are completed. The power unit will remain off after an under voltage condition until the start button is pressed.

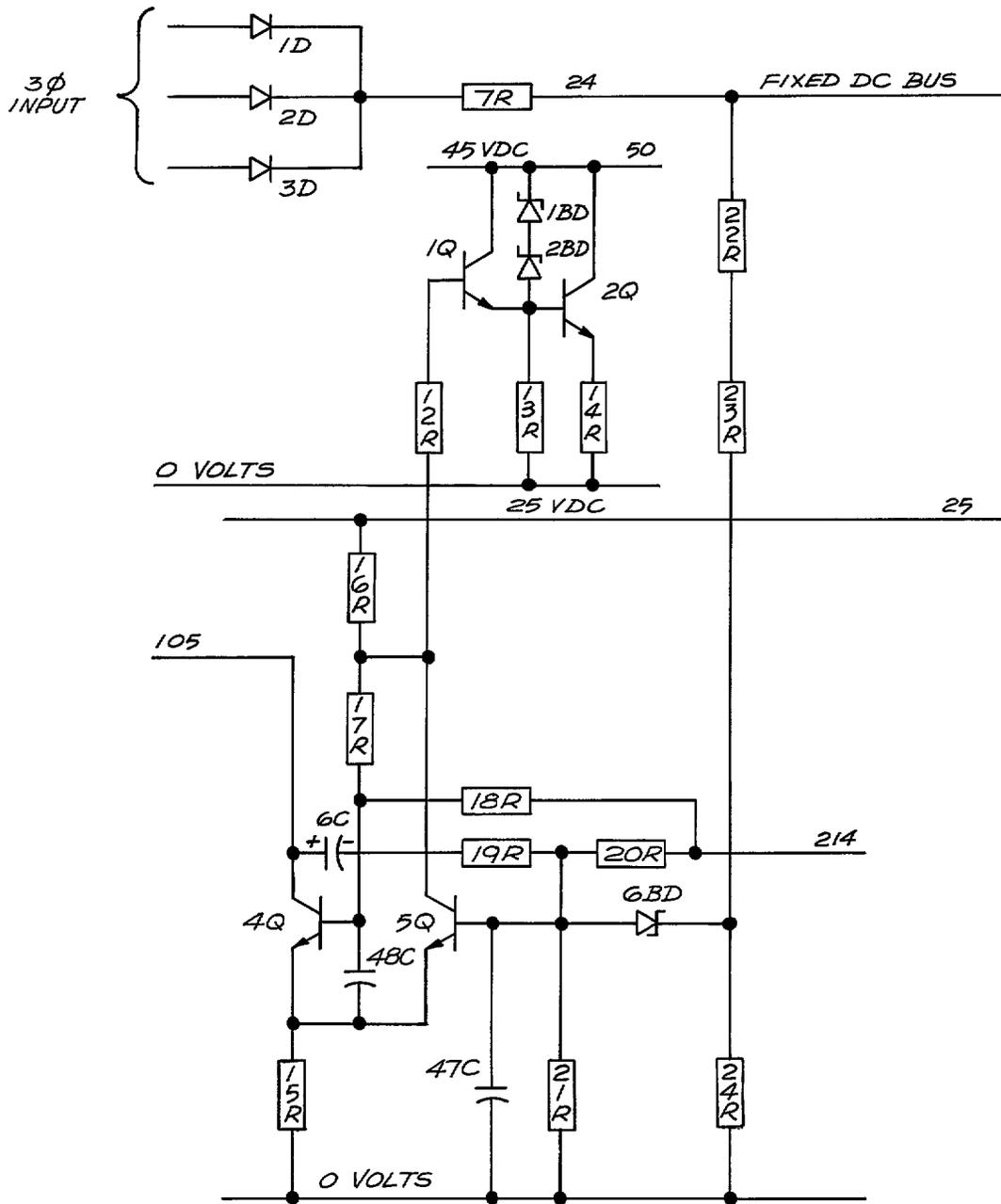


Figure 17. Under Voltage Trip Circuit

## NOTES

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