GATE DISTRIBUTION AND STATUS BOARD

DS200FCGD1A

CONTENTS

Safety Symbol Legend ................................................1
Functional Description................................................1
  Introduction............................................................. 1
  Board Functions.................................................... 1
Application Data ......................................................... 3
  Renewal/Warranty Replacement............................... 6
  Board Identification ..................................................6
  Warranty Terms ........................................................ 6
  Warranty Parts And Service......................................7
  Procedure For Replacing Boards............................... 7

SAFETY SYMBOL LEGEND

WARNING Indicates a procedure, practice, condition, or statement that, if not strictly observed, could result in personal injury or death.

CAUTION Indicates a procedure, practice, condition, or statement that, if not strictly observed, could result in damage to or destruction of equipment.

NOTE Indicates an essential or important procedure, practice, condition, or statement.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The Gate Distribution and Status Card (FCGD) is an interface board for a 6-pulse phase-controlled non-reversing bridge. It receives SCR firing information from the DS200DSPC (DSPC – the VME processor) board and returns feedback and diagnostic information via the VME backplane. The FCGD decodes and distributes cell gating signals for each bridge leg and receives a multiplexed cell status signals from each bridge leg. It also receives and scales bridge feedback signals then sends this voltage, frequency, and current status information back to the DSPC board.

The FCGD board is 6U VME size (9.2x6.3 inches), with six layers and surface-mounted devices (SMDs) on both sides. The FCGD mounts in the same VME rack that houses the Digital Signal Processing Card (DSPC).

BOARD FUNCTIONS

System Clock

To generate firing commands and time stamping feedback values, the FCGD has a system clock register. This is a 16-bit up-counter that rolls over to 0 when it reaches the hexadecimal number 0FFFFH.

LEM is a registered trademark of LEM USA Incorporated.
System Reset

The system reset signal sets all of the registers on the board to their initial values during power up or hardware resets.

System Heartbeat

The heartbeat is a periodic signal generated by an electronic component to announce that the component is still functional. The system heartbeat register on the FCGD supports this function. When written to by the VME host CPU the first time, the board-level heartbeat begins to count at the same rate as the system clock, and a green board-front LED labeled IMOK (I am okay) is lit.

If the number (≈ 8 msec) in the heartbeat register exceeds its design limit, the board front IMOK light and the gating are both turned off. A hard reset is required to exit this condition.

Firing Commands

The fiber-optic firing signal transmitters are controlled by a firing mask register containing six entries corresponding to the six cell strings in a bridge. The FCGD can turn-on up to six fiber-optic transmitters at one time. The contents of the firing mask register may be written directly by the host CPU over the VME bus connection.

Cell Status Feedback

The FCGD receives feedback signals through fiber-optic connections from three FPGA boards. The feedback consists of two sets of leg cell status signals plus the power supply status signals combined into a single 16-bit value. This information is stored in a cell status register.

Zero-crossing Time Detection

Three zero-crossing signals are developed in analog/digital hardware on the FCGD. Each of the three signals controls a digital latch. At each edge of a zero-crossing signal, the value of the system time clock is written into its respective 16-bit register.

VCO Feedback Count Accumulation

Eight voltage-controlled oscillator (VCO) signals are generated on the FCDG. Each of these signals feeds into a 16-bit up-counter. Upon receipt of a command from the VME host CPU the VCO accumulator values are written into eight registers. Also the value of the system time clock is written into the feedback time register.

Voltage Feedback From NATO

The FCGD accepts input signals from the Voltage Feedback Scaling (NATO) board over a 20-pin ribbon cable (see Table 5). These signals include five attenuated analog voltage signals which correspond to plus/minus dc, and three ac voltages all referenced to ground through a local resistor. The input range is rescaled using the jumpers on NATO to keep the resulting signals within the ±10 V range of the signal electronics. Testpoints for the Va, Vb, Vc, Vp, and Vn signals are available on the VME backplane.

Current Feedback

Current feedback is provided by two Current Transformers (source side) or two LEM® modules (load side) located on phases A and C of the power bridge. Conditioning of the current signals yields IA, IB, and IC signals with IA and IC feeding VCO feedback circuits. The circuit minimizes offset drift over time and temperature. IA and IC current signals feed board-front testpoints.

Hardware Overcurrent

The three current signals, combined to form an IFB signal, drive a hardware overcurrent detector. The overcurrent level is set with potentiometer OC_SP on the front of the board (see Figure 2). The IFB signal is compared against this overcurrent level. If IFB is greater than the overcurrent setting for approximately 26 milliseconds, the FCGD causes an overcurrent signal that can only be cleared by a hardware reset.

The IFB signal level can be read at the board front testpoint (OCSP). The red LED lamp on the board front labeled OC indicates operation of the overcurrent protection when lighted.

The hardware overcurrent signal drives an open circuit bussed line on the P2 connector. There are separate bus lines from source and load FCGDs to a processor board (such as the DSPC) because load and source isolators do not necessarily have same sequencing. This signal is also used by the processor board for trip relay. On some processor boards, it is possible to select by means of a
jumper whether the relay or driver energizes or de-
energizes when a fault condition occurs. This is neces-
sary to satisfy the diverse fail-safe requirements of
varying components.

Hardware Flux Calculation
Reconstructed flux signals (FBAR, FCBR, FACR) are
generated in hardware. Though only two go through the
VCO, all three are needed for the zero-crossing detec-
tion.

Analog/Digital Conditioning
Voltage controlled oscillators are used for analog feed-
back of voltage, current, and flux. The VA, VB, VC,
VDC, IA, IC, FLUXBAR, FLUXCBR signals (see Ta-
ble 1) drive the VCOs. The voltage and current signals
also feed into six Sigma-Delta converters which operate
in parallel with the VCOs.

Commutation Failure Signals
The hardware signals for detecting current in a leg are
compared against the actual legs being asked to fire
from the firing mask. Leg current should only be pres-
ent during its gating interval plus the commutation
overlap time. A commutation failure circuit checks that
the leg current is not on during other parts of the cycle.

A load-side commutation circuit checks for a positive
di/dt leg current after the end of its gating interval.

Both of these commutation circuits are combined for
each leg and sent to the FPGA where they increment a
counter. The software can read this counter for exces-
sive time counts and take any necessary action. The
goal is to detect and correct any problem within 15 de-
grees, thereby minimizing the effect on the dc link reac-
tor and load. The counter is reset to zero on each new
firing mask.

Groundfault Protection Signals
The groundfault detection function is implemented in
software.

Difference Current Detection
The source-to-source or load-to-source current differ-
ence function is implemented in software.

Board Selftest
Most of the board functions can be tested on command
from the VME host CPU. The selftests include loop-
back tests and the injection of test signals into analog
signal paths.

APPLICATION DATA

CTLN1
Existing drive products have a 24 V dc hardware loop
(CTLN1) to block gating of cells independent of the
host CPU. These signals are translated into 5 V dc sig-
nal-level voltage and brought into the FCGD through
bussed lines on the P2 VME connector (see Table 5). If
24 V dc on CTLN1 is not present firing is inhibited.

VME Bus Interface
The FCGD board is compatible with the VME
(A24/D16) bus specification both electrically and
physically. The FCGD environment consists of up to
four FCGD boards and a VME bus host CPU. All bus
signals are contained on the P1 connector and the board
decodes most of the 24 address bits for internal addressing. The P2 connector is available as an I/O signal ex-
pansion path and as a means to connect signals between
FCGD boards. The VME bus address of each FCGD
board is set automatically using data provided through
the pins on connector P2. If FCGD boards are relocated
on the bus, each can discover its new address without
operator intervention.

Hardware OC Setpoint Potentiometer
Set the overcurrent level manually for each FCGD
board using potentiometer OC_SP on the board front
(see Figure 2). If the position of a FCGD board in the
VME rack is changed, its overcurrent level needs to be
manually re-adjusted. Compute the OC_SP voltage
level setpoint as follows:

\[
\text{Source-side} : \quad \text{OC}_{-}\text{SP} = \frac{(T.L. \times 1.2825 \times \text{Im} \times 0.6)}{\text{CT}} \\
\text{Load-side} : \quad \text{OC}_{-}\text{SP} = \frac{(T.L. \times 1.2825 \times \text{Im} \times 0.605)}{\text{LEM}}
\]
### Table 1. Testpoints

<table>
<thead>
<tr>
<th>Name</th>
<th>Nomenclature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TP1</td>
<td>VDC</td>
<td>Bridge DC link voltage – attenuated</td>
</tr>
<tr>
<td>TP4</td>
<td>VBA</td>
<td>Bridge line-to-line voltage feedback – attenuated &amp; scaled</td>
</tr>
<tr>
<td>TP5</td>
<td>VCB</td>
<td>Bridge line-to-line voltage feedback – attenuated &amp; scaled</td>
</tr>
<tr>
<td>TP6</td>
<td>VAC</td>
<td>Bridge line-to-line voltage feedback – attenuated &amp; scaled</td>
</tr>
<tr>
<td>TP7</td>
<td>FBAR</td>
<td>Scaled, reconstructed flux. 4.75 V = 1 P.U.</td>
</tr>
<tr>
<td>TP8</td>
<td>FCBR</td>
<td>Scaled, reconstructed flux. 4.75 V = 1 P.U.</td>
</tr>
<tr>
<td>TP9</td>
<td>FACR</td>
<td>Scaled, reconstructed flux. 4.75 V = 1 P.U.</td>
</tr>
<tr>
<td>TP11</td>
<td>IFB</td>
<td>Pseudo -dc link current – unscaled</td>
</tr>
<tr>
<td>TP12</td>
<td>OC_SP</td>
<td>Overcurrent setpoint (26 msec filter) – compared to IFB</td>
</tr>
<tr>
<td>TP19</td>
<td>IA</td>
<td>Phase line current feedback – scaled. 3 V pk = 1 P.U.</td>
</tr>
<tr>
<td>TP20</td>
<td>IC</td>
<td>Phase line current feedback – scaled. 3 V pk = 1 P.U.</td>
</tr>
<tr>
<td>TP21</td>
<td>0FC1</td>
<td>0 = fire cells in leg 1</td>
</tr>
<tr>
<td>TP27</td>
<td>ACOM</td>
<td>Analog signal common (ground)</td>
</tr>
<tr>
<td>TP33</td>
<td>0FC3</td>
<td>0 = fire cells in leg 2</td>
</tr>
<tr>
<td>TP35</td>
<td>0FC5</td>
<td>0 = fire cells in leg 3</td>
</tr>
</tbody>
</table>

### Table 2. Fiber-optic Connectors

<table>
<thead>
<tr>
<th>Name (Color)</th>
<th>Nomenclature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>U56 (Blue)</td>
<td>STAT1 IN</td>
<td>Fiber-optic receiver; cell status feedback from FGPA board</td>
</tr>
<tr>
<td>U57 (Blue)</td>
<td>STAT2 IN</td>
<td>Fiber-optic receiver; cell status feedback from FGPA board</td>
</tr>
<tr>
<td>U67 (Blue)</td>
<td>STAT3 IN</td>
<td>Fiber-optic receiver; cell status feedback from FGPA board</td>
</tr>
<tr>
<td>U71 – U76 (Gray)</td>
<td>LEG1 – 6</td>
<td>Fiber-optic transmitters; firing signals to FGPA board</td>
</tr>
</tbody>
</table>

### Table 3. LED Functions

<table>
<thead>
<tr>
<th>Name</th>
<th>Nomenclature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS1</td>
<td>OC FLT</td>
<td>Red LED indicates when lighted that overcurrent protection is active</td>
</tr>
<tr>
<td>DS2</td>
<td>IMOK(T) ACTIVE</td>
<td>Green LED indicates when lighted that board is functional</td>
</tr>
</tbody>
</table>

### Table 4. Removable Programmable Parts

<table>
<thead>
<tr>
<th>Name</th>
<th>Nomenclature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>U7</td>
<td>EPROM</td>
<td>Serial configuration XC17256D</td>
</tr>
</tbody>
</table>

### Table 5. Onboard Connectors

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>P2</td>
<td>96-pin board-edge connector. Used to set board VME address and for I/O signal routing. Not intended for customer use.</td>
</tr>
<tr>
<td>TSTP1</td>
<td>Connector for 20-pin ribbon cable. Not intended for customer use.</td>
</tr>
</tbody>
</table>
Figure 1. FCGD Board Layout
RENEWAL/WARRANTY REPLACEMENT

BOARD IDENTIFICATION

A printed wiring board is identified by an alphanumeric part (catalog) number stamped on its edge. For example, the FCGD is identified by part number DS200FCGDG#. Figure 3 describes each digit in the part number.

<table>
<thead>
<tr>
<th>DS 200 FCGD G# A A A</th>
</tr>
</thead>
<tbody>
<tr>
<td>LEDS</td>
</tr>
</tbody>
</table>

**NOTE**

All digits are important when ordering or replacing any board.
WARRANTY TERMS
The GE Motors & Industrial Systems Terms and Conditions brochure details product warranty information, including the warranty period and parts and service coverage.

The brochure is included with customer documentation. It may also be obtained separately from the nearest GE Sales Office or authorized GE Sales Representative.

WARRANTY PARTS AND SERVICE
This board has no fuses or other end-user serviceable parts. If it fails, it needs to be replaced as a unit.

To obtain a replacement board, or service assistance, contact the nearest GE Service Office. Please have the following information ready to exactly identify the part and application:

• GE requisition or shop order number
• LCI serial number and model number
• Board number and description

PROCEDURE FOR REPLACING BOARDS

1. Turn off power.
2. To remove the FCGD board, carefully disconnect all cables, as follows:
   – For fiber-optic connectors, press the latch on the mating cable connector. Pull the connector only; do not pull the fiber-optic cable.
3. Install the new FCGD board.
4. Reconnect all cables, ensuring that each connector is properly seated at both ends.

NOTE
Because of upgrades, boards of different revision levels may not contain identical hardware. However, GE Motors & Industrial Systems ensures backward compatibility of replacement boards.

CAUTION
To prevent equipment damage, do not remove boards or connections, or re-insert them, while power is applied to the drive.

Treat all boards as static-sensitive. Use a grounding strap when changing boards and always store boards in anti-static bags or boxes they were shipped in.

To replace an FCGD board:

To prevent electric shock, turn off power to the board, then test to verify that no power exists in the board before touching it or any connected circuits.