OBSOLETE

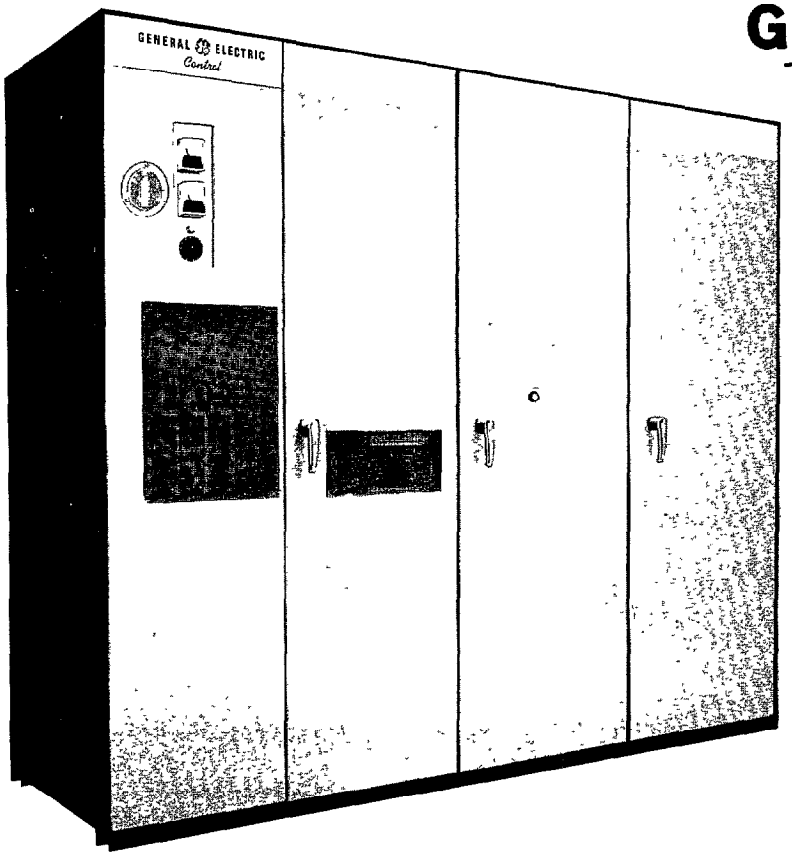
SILTROL* I

IC 3610 Integrated Static Conversion and Control Equipment for Adjustable-Speed Drives

*TRADEMARK OF GENERAL ELECTRIC CO.

INSTRUCTIONS

GEK - 28543A



These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

GENERAL ELECTRIC

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SAFETY PRECAUTIONS

During installation and maintenance all power sources should be removed.

Adjustment or testing of energized circuits should be done only by authorized persons who are familiar with hazards involved.

SILTROL I

SECTION I THYRISTOR POWER SUPPLIES

INTRODUCTION

These instructions apply to reversing and nonreversing, adjustable voltage Thyristor power supplies, of the Siltrol I line.

Before installing, operating, or maintaining this equipment, read these instructions carefully. For specific ratings, relay settings, lineup arrangements and other data, consult the nameplate and the elementary diagrams supplied with the equipment.

GENERAL INSTRUCTION

Installation consists of unpacking, setting up the apparatus, and making connections between the various assemblies. A few suggestions are given here. However, the actual methods used are dependent upon the local conditions existing at the time of installation.

Receiving, Unpacking and Storage

This equipment is assembled, tested and packed with care to enable the purchaser to install and place it in operation with a minimum of time and labor. Immediately upon receiving the equipment, it should be carefully checked against the memorandum of shipment. If any parts are found damaged or missing, the purchaser should immediately present a claim to the Transportation Company and notify the nearest sales office of the General Electric Company.

It is good practice to place the equipment as near as possible to its permanent location before unpacking. The standard type of unpacking tools should be used. A nail puller can be especially useful. Careless unpacking methods will invariably result in parts being damaged or marred. Some parts such as bolts and screws are packed in special containers to keep them together; however, they may become separated. Therefore, packing material should not be discarded until it is certain that all parts have been removed. Equipment should be thoroughly cleaned to remove particles of packing material or foreign substances which may have become lodged in or between any of the parts. Apparatus not immediately installed should be labeled and set aside in a clean dry place of moderate temperature and protected from injury.

Locations and Connections

When equipments are installed, ample space should be provided around the various parts to permit easy inspection, adjustment and repair. Whenever possible all control devices are mounted at the factory; interconnections are made and leads are brought out to numbered terminals, making it necessary only to install the component pieces and connect the numbered terminals to the various pieces of apparatus. The interconnection diagrams supplied should be used as a guide for making the connections.

When the equipment has been set up, it should be thoroughly inspected and checked to be sure that all connections are complete and tight, that the relays and instruments are in good mechanical condition, that they have been thoroughly cleaned, and that all of the movable parts work freely. All devices should make good contact and have clean surfaces. Special care should be taken to insure that the printed circuit cards make good contact at the rear of the page assembly.

MAINTENANCE

Inspection Routine

A periodic routine of cleaning and inspection should be established. Such cleaning is necessary to prevent faulty operation of a device due to accumulation of dust and corrosion. Inspections should be more frequent when the demands on the equipment are exacting. Under normal conditions, the protective devices do not operate; therefore, these devices need careful inspection. If the equipment is in operation when being inspected and a short interruption of service can be permitted, the manual tripping of a protective device will afford an opportunity to observe the manner in which the equipment is functioning.

If at any time a device fails, the cause of the failure should be determined at once. The remedy should be applied and if necessary the part should be adjusted or replaced.

WHEN ORDERING PARTS, GIVE A DETAILED DESCRIPTION OF THE PART AND COMPLETE NAME-PLATE DATA ON THE DEVICE.

For specific maintenance information on the various devices refer to the particular instruction book. Under no circumstances should an automatically controlled equipment be started by hand until the cause of the failure to start automatically is determined and corrected.

Records and Log Book

It is recommended that a regular inspection and maintenance program be employed and that a log book be kept. This procedure will help detect malfunctioning equipment and determine causes of trouble.

EQUIPMENT CONSTRUCTION AND DESCRIPTION

General Description

Siltrol I is an integrally built combination of power conversion and control equipment designed for d-c adjustable-speed motor drives. The power conversion is achieved via thyristors converting customer a-c supply to an adjustable d-c voltage.

Because of modular construction techniques the Siltrol I equipment is compact and can be arranged in many physical configurations to meet a variety of installation requirements. Integrated construction means that interconnection of conversion equipment and control is done in the factory reducing installation time and cost. In addition, installation check-out time is reduced because integrated equipments facilitate more complete factory tests.

Siltrol I equipments are constructed in three basic sizes:

Small HP nominal rating (5-25 HP) at 500 V.
Medium HP nominal rating (25-400 HP) at 500 V.
Large HP nominal rating (400-800 HP) at 500 V.

Small HP

The small HP version covers the nominal ratings 5-25 HP where the power conversion equipment and drive regulator are mounted in a 36" wide unit. Whenever possible the line panel and control relays are also mounted in the same unit. For the nominal ratings (5-25 HP) the unit is convection cooled.

Medium HP

The medium HP version covers the nominal ratings 25-400 HP where the power conversion equipment and drive regulator are normally mounted in a 48" wide unit. The line panel and control relays are housed in separate units which are integrated with the power conversion unit in various configurations such as side-by-side and back-to-back. The power conversion unit is force ventilated.

Large HP

The large HP version covers the nominal ratings 400-800 HP and utilizes two power bridges connected in parallel. The power bridges are mounted in a 48" unit and the isolation transformer, breaker, line panel and control relays, etc., are mounted in separate units.

Each power converter consists of the following basic components:

a) Incoming line breaker - The breaker, together with the protective circuits, provides overcurrent and short circuit protection to the converter isolation transformer and provides a means for main incoming power disconnect.

b) Converter isolation transformer, open dry type, air cooled, with thermal switch in the winding and ± 5% primary taps.

c) Thyristor 3 phase double way bridge rectifier assembly with 6 controlled legs. The complete rectifier circuit consists of thyristor cells mounted on aluminum heat sinks, with dry type reactors and current limiting fuses in each leg of the bridge circuit. R.C. circuits are connected, in parallel, with each cell. For reversing converters the forward and reverse rectifier circuits are included in the same assembly.

d) Current transformers, window type, encapsulated for protection.

e) Firing circuit module containing circuitry necessary for gate pulse generation lock out logic, current signals, etc., utilizing Directo-Matic II plug-in printed circuit board construction.

f) Gating modules containing gate pulse transformers and associated components, utilizing DOM II plug-in printed circuit board construction. The gating modules also house the cell indicating lights.

g) Auxiliary control, including control power transformers and auxiliary relays.

h) Ventilation system for once-through cooling with three phase motor driven blower, motor protection, loss of air detection (air flow switch) and the necessary ducts and baffles.

NOTE: All components and assemblies are accessible and removable from the front of the unit through full height hinged doors. Access to the power bus is through removable panels at the rear.

ELECTRICAL DESCRIPTION OF OPERATION

1. POWER CONVERSION

The function of changing a-c power to adjustable voltage d-c power is made possible by the ability of thyristors to block voltage in both directions while the degree of current flow in one direction is controlled by "gating" the thyristors at different phase angles on the a-c voltage wave. The three phase bridge rectifier circuit produces six phase ripple on the d-c bus.

The complete converter circuit consists of one (or two paralleled-large HP) 3 phase full wave bridge circuit with the thyristors mounted on air cooled heat sinks. Dry type reactors and current limiting fuses are connected in series with each cell leg of the bridge to provide protective and operational functions. Cell monitor lights provide visual indication of the condition of each thyristor during operation. Figures 1 and 2 show thyristor bridge circuits for non-reversing and reversing drives respectively.

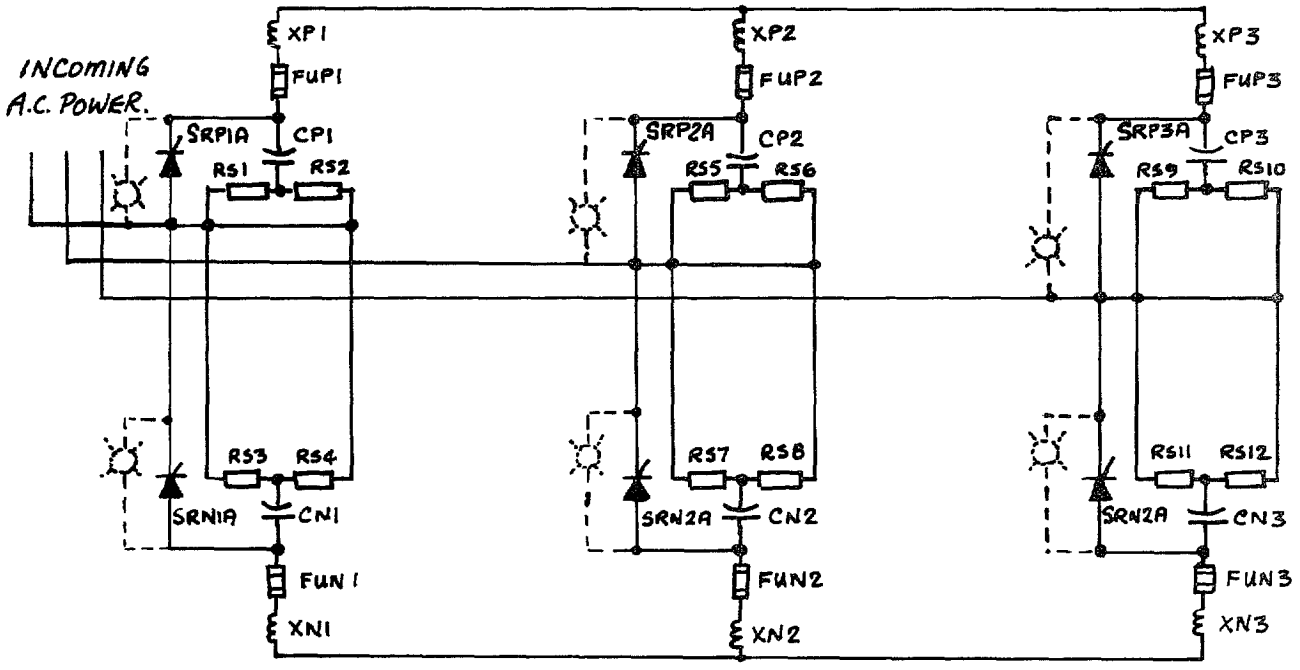


Figure 1 - Non-reversing Thyristor Power Circuit

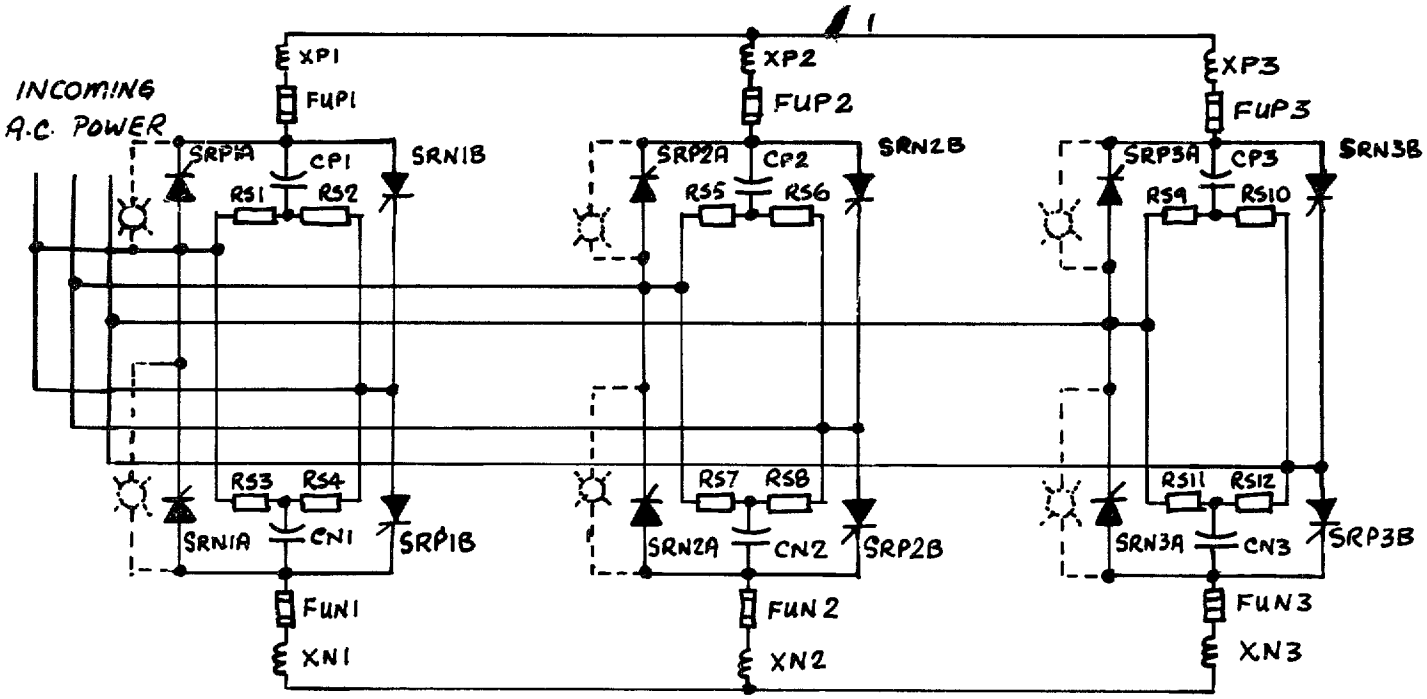


Figure 2 - Reversing Thyristor Power Circuit

An isolating type rectifier transformer when used is specifically designed to coordinate with the rectifier for proper circuit and regulation characteristics; provides isolation from grounds and surges; and limits available fault currents. The transformers are normally wound either delta-wye or delta-delta for rectifier circuits USAS-23 or USAS-25 respectively.

The standard power transformer is dry type, with one plus 5% and one minus 5% primary taps and with overtemperature detectors.

Various modifications are available including:

Primary taps 1+2-1/2% and 1-2-1/2%.
Primary taps 2+2-1/2% and 2-2/1/2%.
No primary taps (nominal connections only).

2. FIRING CIRCUIT

(A detailed description of operation of the firing circuit is given in Section 2 of the Instruction Book and a brief description only is given here).

The output d-c voltage of the rectifier bridge is regulated by continuous adjustment of the time in the power cycle at which the thyristors are gated. This voltage regulating function is accomplished by the use of biased cosine control.

Figure 3 is a simplified block diagram of the firing circuit for a reversing Siltrol I control and shows the principle of operation.

Referring to Figure 3 the various inputs to the firing circuit are as follows:

a) Six Phase Reference

The reference sine waves are derived from a 3 phase 50/60 cycle phasing transformer whose primary is normally connected in delta and secondary in 6 phase star. These secondary windings give the 6 reference waves and are conditioned for use in the firing circuit in a phase shift line filter.

b) Current Signals from CT's

The a-c lines which feed the A and B thyristor bridges are each fed through current transformers, 3 for the A bridge and 3 for the B bridge. Their function is to indicate the level of current in each bridge. As the outputs of the CT's are a-c they are rectified in an ACCT Rectifier circuit. This circuit consists of 2 full wave bridges one each for A and B, producing d-c voltages (IA or IB).

IA and IB are used in the following ways:

(i) Generation of I_L (Process control current feedback).
(ii) Static overcurrent protection.
(iii) Lockout circuitry
(iv) Circulating current protection.
(v) Retard limit ontrol.

c) VIA

VIA is a voltage proportional to the thyristor bridge d-c output voltage. The signal is obtained from the output of an isolation amplifier whose input is connected to the Siltrol output terminals.

d) REF 1

REF 1 is the input signal from the process control and ranges between

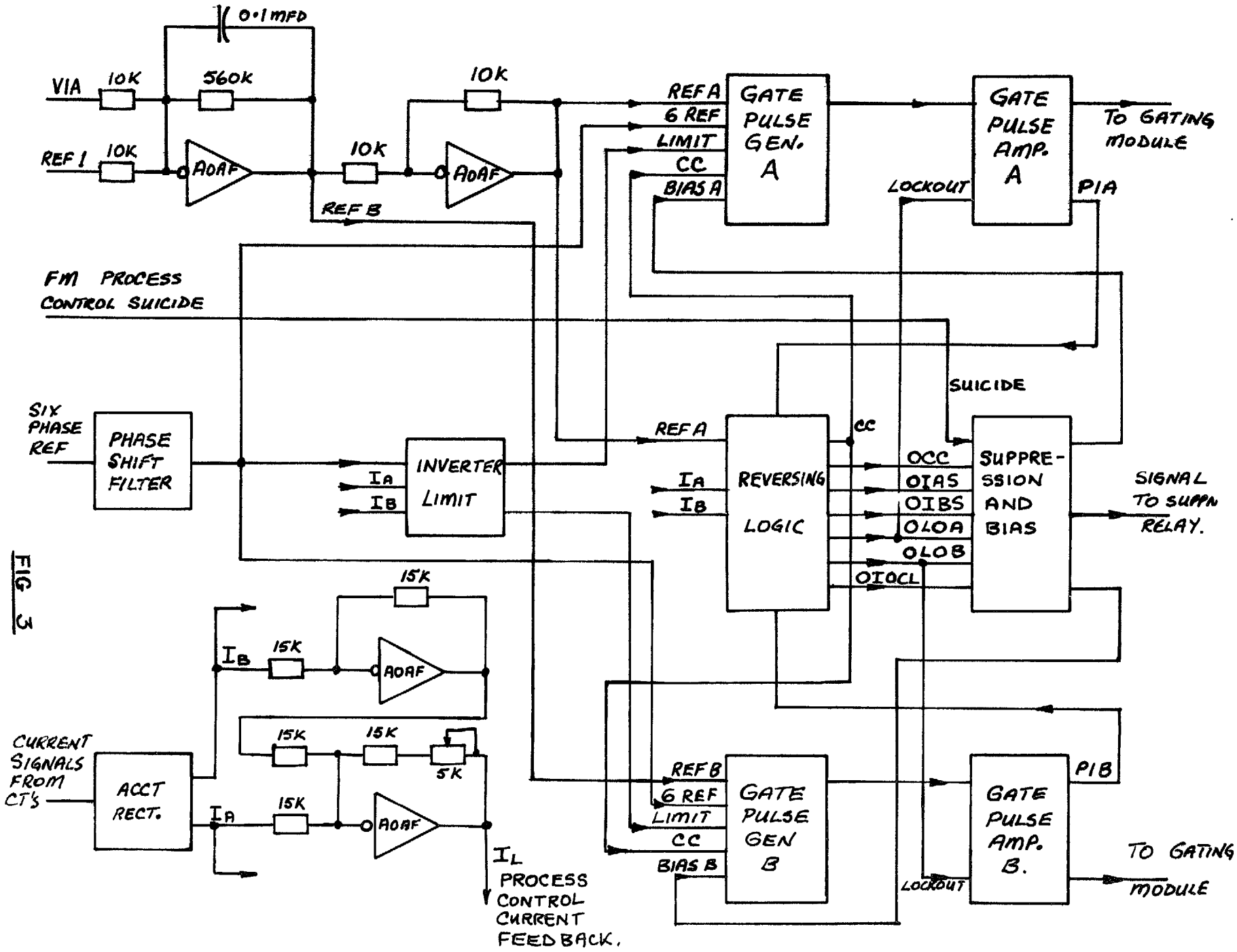

0·1 MFD
VIA
10K
560K
REF 1
10K
AOAF
10K
REF B
10K
AOAF
REF A
6 REF
LIMIT
CC
BIAS A
GATE PULSE GEN. A
GATE PULSE AMP. A
TO GATING MODULE
LOCKOUT
PIA
FM PROCESS CONTROL SUICIDE
SUICIDE
SIX PHASE REF
PHASE SHIFT FILTER
INVERTER LIMIT
IA
IB
REF A
IA
IB
REVERSING LOGIC
CC
OCC
OIAS
OIBS
OLOA
OLOB
OIOCL
SUPPRESSION AND BIAS
SIGNAL TO SUPPN RELAY.
15K
IB
15K
AOAF
15K
15K
5K
CURRENT SIGNALS FROM CT's
ACCT RECT.
IA
15K
AOAF
IL
PROCESS CONTROL CURRENT FEEDBACK.
REF B
6 REF
LIMIT
CC
BIAS B
GATE PULSE GEN B
GATE PULSE AMP. B.
PIB
LOCKOUT
TO GATING MODULE

FIG 3

± 15 V. This reference is summed with VIA and the error signals produced (Ref. A & Ref. B) are summed with the reference sine waves in the gate pulse generators. The gate pulse generators produce timing pulses which via the gate pulse amplifiers and gating modules fire the proper thyristor at the proper time to produce the desired output voltage.

e) Process Control Suicide

The process regulator suicide signal initiates a bias signal to both the A and B gate pulse generators to retard firing pulses to a retard limit. In addition a 100 resistor is connected around the gain and stabilization amplifier via a suicide relay.

f) Inverter Limit

The inverter limit input to the gate pulse generator controls the maximum retard limit angle when inverting to ensure good inter-cell commutation. The inverter limit circuit controls the retard limit as a function of current and voltage, to compensate for the increased commutating angle at higher currents.

g) Reversing Logic

The function of the reversing logic circuit is to monitor IA, IB and REF A to decide what lockout conditions should be. It is designed to (1) lock out either or both A and B package by inhibiting pulses in the gate pulse amplifier; (2) cause either or both thyristor bridges A and B to phase back to retard limit; (3) cause a relay driver circuit to shut the drive down.

The reversing logic circuit provides the necessary logic to ensure that, if no current is flowing, the polarity of REF A determines which side is locked out. If current is present in one package, the current signal overrides the reference signal and locks out the other bridges. If current is present in both bridges a circulating current fault condition is detected and both gate pulse generator outputs are phased back to retard limit and both pulse amplifiers locked out.

The circuit also monitors the level of IA and IB, and provides two levels of overcurrent protection. The first level via the bias and suppression circuit phases back the correct thyristor bridge to maximum retard, and initiates a process control fault stop.* By connections on a co-ordination card the condition can either be automatically reset when current returns to zero or require manual reset. A higher second level overcurrent will generate a suppression alarm and phase back both bridges to maximum retard and initiate a process control fault stop.* This condition must be manually reset.

3. PROTECTIVE FEATURES

(a) Transformer Fault -- Trips a-c circuit breaker or primary interrupting device and initiates process control fault stop.* Operator must reclose breaker after correction of the fault condition.

(b) Transformer Overtemperature -- Temperature detectors are available to provide whatever protection customer requires.

(c) Static DC Overcurrent Protection -- Protection is provided for two overcurrent levels with the following settings and features. As an example consider a drive with a maximum current rating of say 300% for 10 seconds.

The first level overcurrent is set to operate at 1.1 x 300%. The second level operates at 1.2 x the first level setting = 1.2 x 1.1 x 300%. Both levels operate the suppression relay, phase firing pulses to retard limit, and initiate a process control fault stop.* If the fault is first level the suppression relay is reset automatically after removal of fault current. However the auto reset feature can be eliminated by connections on a coordination card.

If the fault is second level, then the condition must be manually reset at the panel.

If a circulating current condition exists (i.e. more than 2% current in both A and B bridges simultaneously) all pulses are suppressed via lockout, the suppression relay operated and a process control fault stop initiated.* This condition must also be manually reset.

(d) Loss of Cooling -- Insufficient cooling detected by air flow switch or heat sink overtemperature device, initiates a process control fault stop.*

(e) Cell Failure -- Suppression circuit locks out cell gate pulses and initiates process control fault stop.* Indication by cell monitor light.

(f) Diode Clipper and Voltage Surge Suppressor -- On primary feeder circuits above 600 volts a three phase bridge diode circuit and surge suppressor unit is applied to clip transient surges below the level which would damage the cells. Clear indicating lamps show normal operation.

* When a process control fault stop is initiated, the control under-voltage circuit will open, the motor line contactor will open, the regulator reference is removed, and the drive will coast to a stop or will be dynamically braked (if used) by applying full field to the motor and closing a dynamic braking resistor across the motor armature.

SECTION II ELEMENTARY DIAGRAMS

Because the Siltrol equipments are basically standard items the elementary diagrams are standardized with variable information being provided on data tables within the elementaries.

To completely describe a particular Siltrol there are four levels of elementary diagrams which are as follows:

LEVEL 1 - Requisition Drive Elementary

Within each requisition drive elementary there are two sheets which describe the Siltrol for that drive:

1) The Symbol Sheet consisting of a symbol functionally describing the Siltrol in block form only, but showing all incoming and outgoing interconnections in detail.

2) The Siltrol Power Convertor Design Variable Data Sheet showing all relevant data for that particular Siltrol. This is presented in the form of a table for each sheet of the Siltrol Power Convertor Elementary, showing all devices and functions, relevant catalog numbers, adjustments, and notes.

LEVEL 2 - Siltrol Power Convertor Elementary

The Level 2 elementary diagrams describe the Siltrol Power Convertor in modular form, with each module represented by a symbol block describing functionally how it works. All wires into each module are shown in detail. The elementary also includes data tables showing variable information. To cover all 6 types of Siltrol equipments produced, there are 6 versions of this elementary. But, only those required to cover the types of Siltrol equipment used in this requisition are included in the Instruction Book.

The six versions are:

Small HP - Non-reversing
Small HP - Reversing
Medium HP - Non-reversing
Medium HP - Reversing
Large HP - Non-reversing
Large HP - Reversing

The Level 2 diagrams are located in Section 2 of this Instruction Book.

LEVEL 3 - Siltrol Module Elementaries

The Siltrol equipment is divided into three modules:

1. Power Bridge Module
2. Firing Circuit Module.
3. Gating Module

1) This elementary shows the power bridge circuit in detail. As the power bridge is ordered by catalog number a complete breakdown of the number is given as part of the elementary.

2) The firing circuit is shown in detail except that each card in the firing circuit module is represented by a symbol which shows functionally how it works. A data sheet is also provided showing possible variations related to catalog number.

3) Similarly the gating module is shown in detail with each card represented by a symbol which shows functionally how it works. Again a data table is provided showing the possible variations related to catalog number.

The Level 3 elementary diagrams are located in Section 3 of the Instruction Book.

LEVEL 4 - Siltrol Card Elementaries

These elementaries describe the various cards used in the Siltrol equipment in detail and consist of:

1. Circuit diagrams
2. Symbol diagrams
3. Application Data

The Level 4 elementary diagrams are located in Section 4 of this Instruction Book.

FIRING CIRCUIT - DETAILED DESCRIPTION

To fully understand the operation of the Siltrol I equipment, a complete understanding of the firing circuit is essential. Fig. 4 shows the Level 2 symbol diagram for a small HP reversing firing circuit. The diagram describes in detail functionally how the firing circuit works.

It is not a circuit diagram.

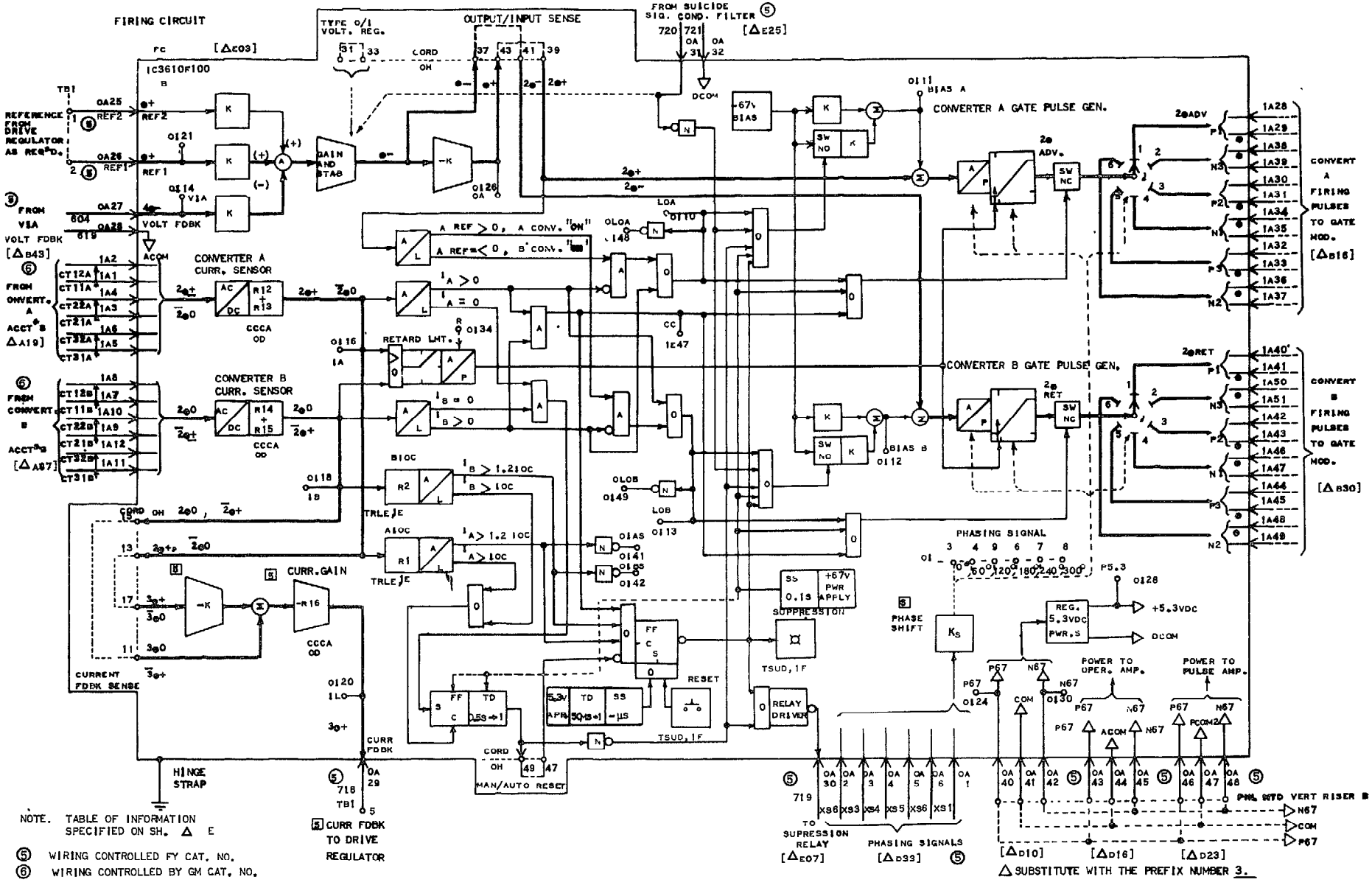
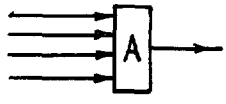
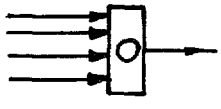
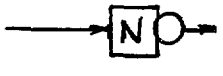

FIRING CIRCUIT
TYPE 0/1 VOLT. REG.
OUTPUT/INPUT SENSE
FROM SUICIDE SIG. COND. FILTER
IC3610F100
REFERENCE FROM DRIVE REGULATOR AS REQ'D.
VOLT FDBK
CONVERTER A CURR. SENSOR
CONVERTER B CURR. SENSOR
CONVERTER A GATE PULSE GEN.
CONVERTER B GATE PULSE GEN.
RETARD LMT.
BIOC
AIOC
TRLEJE
CURR.GAIN
PHASING SIGNAL
PHASE SHIFT
SUPPRESSION
TSUD,1F
RELAY DRIVER
RESET
MAN/AUTO RESET
HINGE STRAP
CURRENT FDBK SENSE
CURR FDBK TO DRIVE REGULATOR
TO SUPRESSION RELAY
PHASING SIGNALS
POWER TO OPER. AMP.
POWER TO PULSE AMP.
REG. 5.3VDC PWR.S
+5.3VDC
DCOM
NOTE. TABLE OF INFORMATION SPECIFIED ON SH. Δ E
WIRING CONTROLLED FY CAT. NO.
WIRING CONTROLLED BY GM CAT. NO.
SUBSTITUTE WITH THE PREFIX NUMBER 3.

Figure 4

Firing Circuit Description (cont'd)

In order to read the symbol diagram it is important that the reader understands how to interpret the basic logic and analog symbols used.

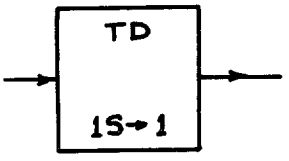
SYMBOL	DESCRIPTION
BASIC LOGIC ELEMENTS	
1. AND 	This symbol represents a logic "AND" element. The symbol, as shown, is to be interpreted as follows: "1's" are required on all four (4) inputs to obtain a "1" output. Conversely, a "0" on one or more inputs will result in a "0" output.
2. OR 	This symbol represents a logic "OR" element. The symbol as shown is to be interpreted as follows: A single "1" at any one of the four (4) inputs is all that is required for a "1" output. Of course, more than one "1" input will also result in a "1" output. Conversely, "0's" on all four (4) inputs will result in a "0" output.
3. NOT (Element)  OR 	This symbol represents a logic "NOT" element. In other words, this is a logic inversion element where the input and output are of opposite states. Although the two symbols perform identical functions, their true states are read differently. The first symbol reads "0" input gives a "1" output. The second reads "1" input gives a "0" output. The selection of which symbol to use is dependent upon which true state makes the diagram more readable.

SYMBOL

DESCRIPTION

BASIC LOGIC ELEMENTS

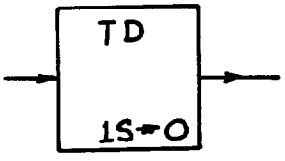
4. TIME DELAY



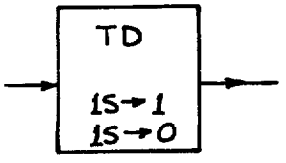
This symbol represents a logic "time delay" element. The first two (2) symbols, as shown, are to be interpreted as follows:

One (1) second after application of a "1" input will result in a "1" output, as indicated by the expression, 1S ⟶ 1.

Other Examples



The time delay may be in the direction of an output "0", as indicated by the expression, 1S ⟶ 0, denoting a one (1) second time delay to "0" output.



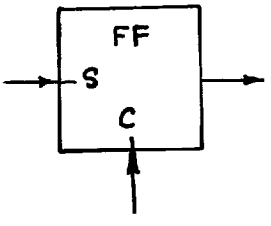
The following abbreviations of the units of time delay should be used:

us = Microsecond
ms = Millisecond
s = Seconds
m = Minutes
h = Hours

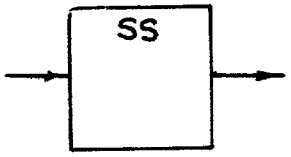
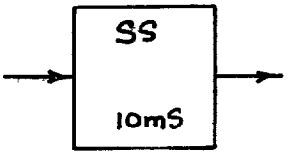
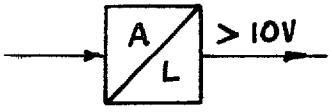
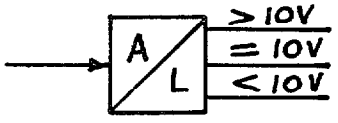
The numeric value and time unit is determined by its application.

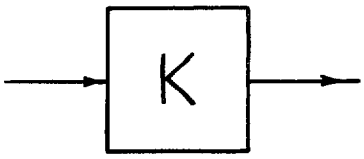
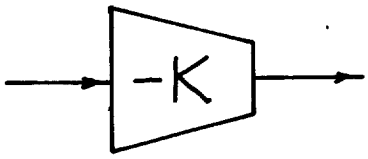
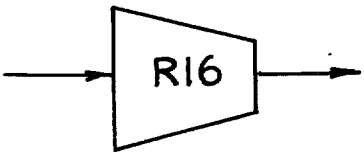
Special Purpose Logic Functions: These are frequently used logic functions which, as a general rule, can be constructed from basic logic elements.

5. FLIP-FLOP



This symbol represents a logic "flip-flop" which is a logic device that has memory or storage properties. By definition, it is a two (2) input device. The S (or "set") input inserts a signal which is stored on output. The C (or "clear") input removes the stored signal output. Furthermore, a "clear" signal input will be preferential over a "set" signal input. The symbol, as shown, is to be interpreted as follows:

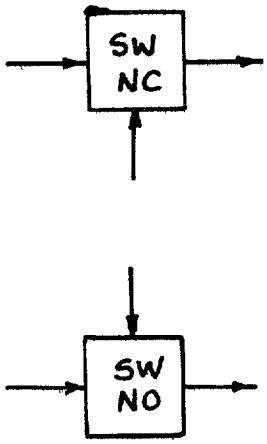
SYMBOL	DESCRIPTION
5. FLIP-FLOP - continued	A "1" on the S (or "set") input will cause a "1" on the output, which will remain "1" when the S input signal is returned to a "0". A "1" on the C (or "clear") input will cause the output to go to a "0", which will remain "0" when the C input signal is returned to a "0". Should a "1" appear simultaneously on both the S and C input terminals, then the output will remain a "0" since the C input always has preference over S input.
6. SINGLE SHOT  	This symbol represents a logic single shot, a logic device that emits a pulse output. The symbol, as shown, is to be interpreted as follows: A "1" input will cause a "1" output pulse. Changing the input to "0" will have no affect on the output. For applications where pulse width is important, its duration should be specified as shown. Use the same units of time for TIME DELAY logic function.
7. ANALOG TO LOGIC CONVERTER  	This represents a logic function that converts an analog input to a logic output in accordance with the expression shown above its output. The first symbol, as shown, is to be interpreted as follows: An analog signal input greater than 10 volts will cause a "1" output. The second symbol as shown is to be interpreted as follows:

SYMBOL	DESCRIPTION
7. ANALOG TO LOGIC CONVERTER (continued)	There will be three (3) logic outputs. One will be a "1" when input greater than 10V; another, a "1" when input equal to 10V; and another, a "1" when input less than 10V. The following signs should be used to express the relationship to a specified analog input: = Equals to <> Not equal to. < Less than. > Greater than. <= Less than or equal to. >= Greater than or equal to.
8. 	This represents a linear transfer function K in which there is no inversion between input and output. Examples: resistors, resistance bridges, non-inverting amplifiers, etc.
9.  	Same as above except that there is an inversion between input and output. Where it is desired to indicate a particular component that affects the gain of a transfer function this symbol is used. It indicates that the gain of the transfer function can be changed by adjustment of R16, not that the gain is R16.

SYMBOL

DESCRIPTION

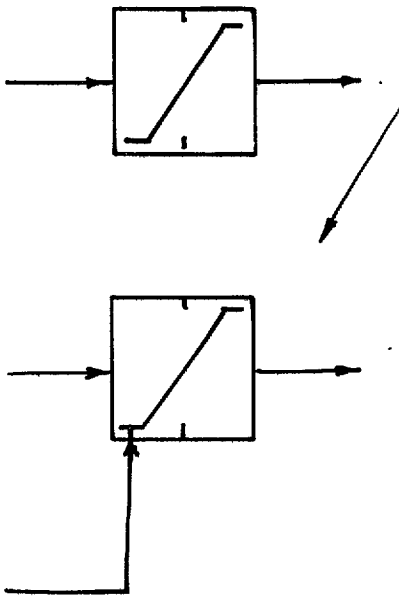
10.



This represents a switch that gates the output signal with respect to its input signal. The input is on the left and the output is on the right. The signal for operating the switch may be shown along the upper or lower side of the box. The letters NC imply that the switch would be closed if the switch operating signal were removed. The letters NO imply that the switch is open under the same conditions.

Examples: interlocks, SCR's, transistors, etc.

11.



Represents a linear transfer function in which the output has positive and negative limits.

This example shows that the negative limit is controlled by another signal.

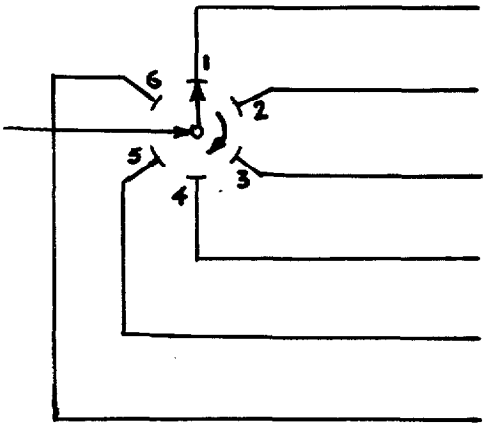
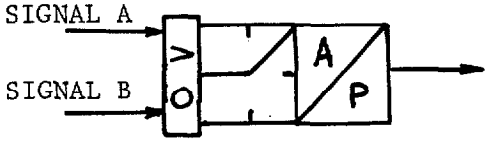
SYMBOL	DESCRIPTION
12. 	This symbol represents the generation of 6 pulses which appear sequentially 1 thru 6.
13. 	This symbol shows the way that various symbols can be combined. It is to be interpreted in the following way: The greater of the two analog signals (signal A and signal B), if positive produces a control signal in the pulse domain.

Fig. 4, Sheet 2-3 showed the complete firing circuit symbol in detail. The following is a breakdown of the firing circuit describing in detail each portion of the symbol:

INTERNAL VOLTAGE REGULATOR:

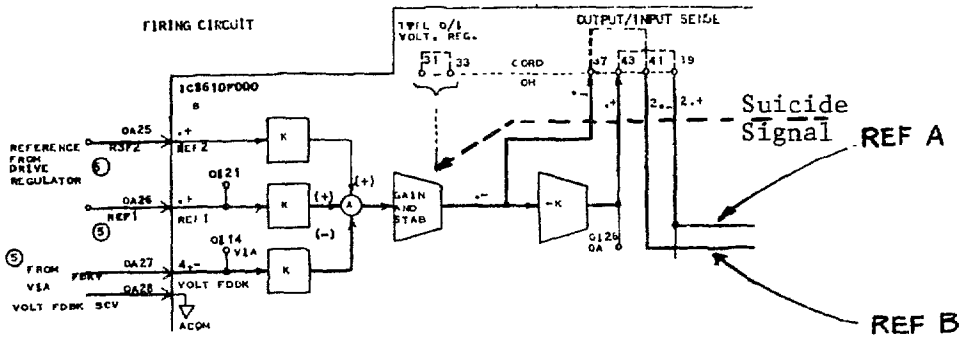


Figure 5

The above portion of the firing circuit symbol shows the generation of the two analog signals, Ref. A and Ref. B, which are applied to the A&B gate pulse generators.

All reversing and some non-reversing Siltrol drives have an internal voltage regulator. The transfer function for the Siltrol for drives with the internal voltage regulator is:

$$\frac{Ed}{15\ [1000]}$$

The first operational amplifier provides the necessary gain and stabilization circuitry and is connected as shown on Figure 6.

The "suicide signal" shows a relationship exists between the suicide signal and the gain and stabilization amplifier. The relationship is that whenever a process regulator suicide signal is present a 100Ω resistor is connected around the amplifier.

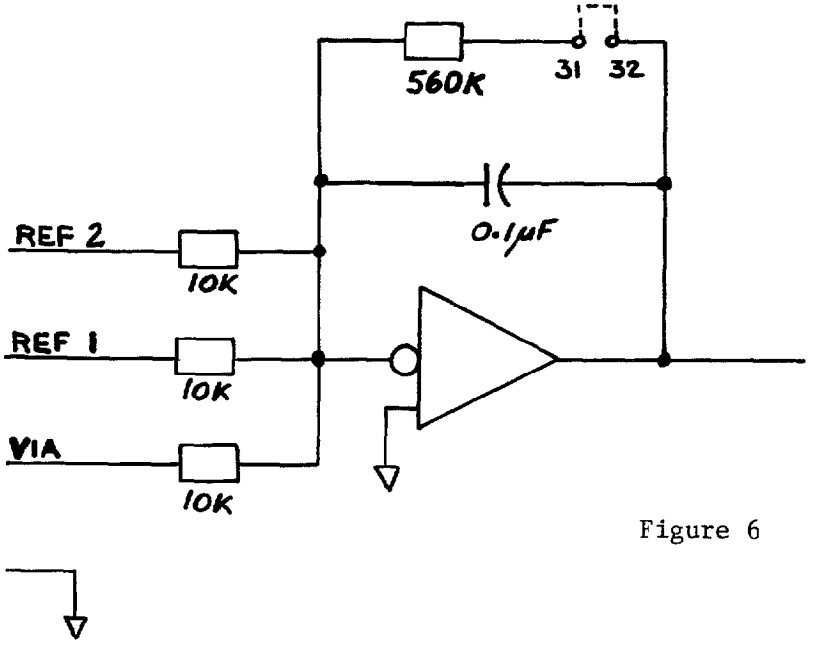


Figure 6

For a type 0 system pins 31 and 32 of the coordination card are jumpered to give the amplifier a finite gain of 56 and a downbreak at approximately 20 radians.

$$\frac{56}{[20]}$$

For a type 1 system, the jumper is not connected and the amplifier has a gain of:

$$\frac{1000}{P}$$

The second operation amplifier has unity gain and simply inverts the output of the first amplifier so that both negative and positive signals (Ref. A & Ref. B) are available to drive A & B gate pulse generators. On a non-reversing drive this amplifier is obviously not required and therefore not provided.

Note on Figure 5 that by connections on the coordination card CORD (Slot 0H), the output/input sense of the Siltrol can be inverted. IF FOR ANY REASON THE INPUT/OUTPUT SENSE OF A SILTROL IS CHANGED THEN THE VOLTAGE FEEDBACK SENSE MUST BE CHANGED BY INTERCHANGING THE CONNECTIONS IN1 & IN2 ON THE VOLTAGE ISOLATION AMPLIFIER VIA.

On some non-reversing applications an internal voltage regulator is not required. In which case, the operational amplifier has a 10K feedback resistor to give unity gain.

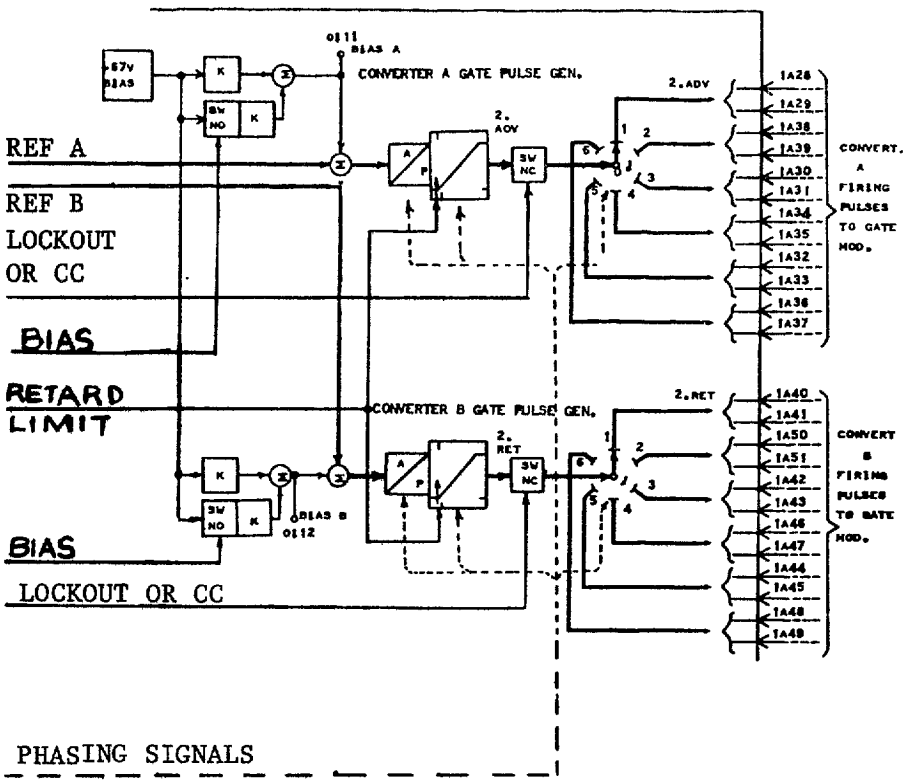


Figure 7

Reference A and Reference B are applied to converters A and B Gate Pulse Generators respectively.

Considering Reference A only, it is summed with Bias A and with 6 sine wave phasing signals to produce 6 firing pulses at the desired phase angle. (The operation of the gate pulse generator is discussed in detail later.)

Similarly, Reference B is summed with Bias B and 6 sine wave phasing signals. (The functions of the signals: Bias Lockout, Circulating Current and Retard Limit signals are discussed in detail later.)

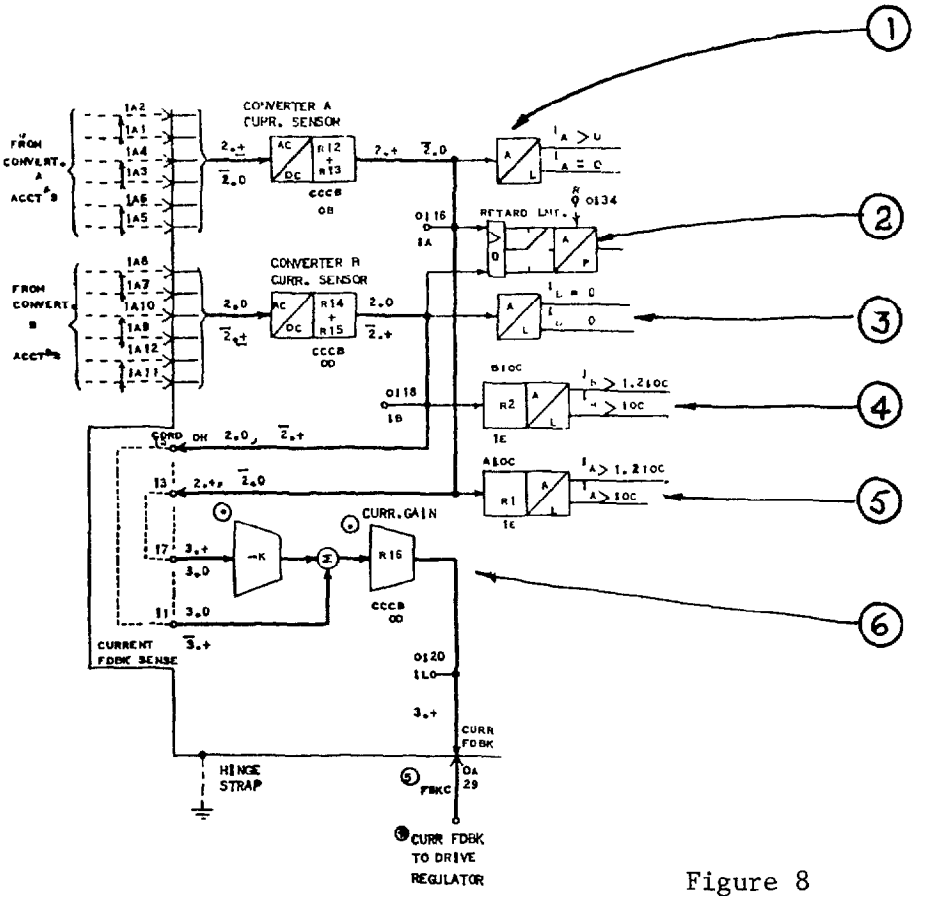


Figure 8

The a-c lines, L1-L2-L3, which feed the A & B thyristor bridges are each fed through a current transformer.

There are 6 CT's employed; 3 for the A bridge and 3 for the B bridge.

The outputs of the CT's are a-c and are rectified in the "AC/DC" "current sensor", as shown in the Figure 8. The nature of the CT is such that a burden resistor is required to attain a specific voltage at a specific a-c line current. These resistors (R12, R13, R14, and R15) are, therefore, selected on a per drive basis to obtain the desired output voltage for rated current.

The d-c output voltages of the A and B current sensors are designated I_A and I_B respectively. These signals are used in the inverter limit circuitry, the reversing logic circuitry and the operational amplifiers to generate the process regulator current feedback (I_L).

Current Feedback (continued) -

To provide the necessary logic signals for the inverter limit and reversing logic circuitry various analog to logic signals are generated as shown in Figure 8 by symbols (1) through (5).

(1) and (3) - These symbols show the generation of two logic signals each from the I_A and I_B analog signals.

$I_A > 0$ - A logic "1" is produced when I_A is greater than 0.

$I_A = 0$ - A logic "1" is produced when I_A is equal to 0.

$I_B > 0$ - A logic "1" is produced when I_B is greater than 0

$I_B = 0$ - A logic "1" is produced when I_B is equal to 0.

(2) - This symbol shows the production of a signal to program the retard limit as a function of I_A or I_B.

(4) and (5) - These symbols show the generation of logic signals produced by overcurrent conditions.

$I_A >$ IOC - This is a logic "1" when I_A is greater than 1 x the overcurrent setting, the level of which is adjusted by R1. IOC level is 1.1 times the maximum rating (e.g. 300% for 10 sec.); IOC level = 1.1 x 300%.

$I_A > 1.2$IOC - This is a logic "1" when I_A is greater than 1.2 x the overcurrent setting; 1.2 x 1.1 x 300%. This level is automatically obtained by adjustment of R1 for the 1.0 overcurrent setting. There is no independent adjustment.

Similarly for package B, logic signal "1's" are obtained for $I_B >$ IOC and $I_B > 1.2$ IOC with adjustment by R2.

(6) - The outputs of A & B current sensors are positive voltages designated I_A and I_B and are used to generate I_L (the drive regulator current feedback signal) via two operational amplifiers. As connected on Figure 8 I_A is fed through a unity gain inverting amplifier and its output ($-I_A$) is summed with I_B. Since I_A and I_B are such that both cannot be present simultaneously, either $-I_A$ or I_B will drive the second amplifier. The gain of the second amplifier is adjustable by R16 on card CCCA slot OD to give the desired output gradient.

With the coordination card connections as shown on Figure 8 and with current flowing in package A, I_L will be a positive voltage. With current flowing in package B, I_L will be a negative voltage. This sense can be inverted by changing the pin connections 15, 13, 17 and 11 on the coordination card.

REVERSING LOGIC AND OVERCURRENT PROTECTION

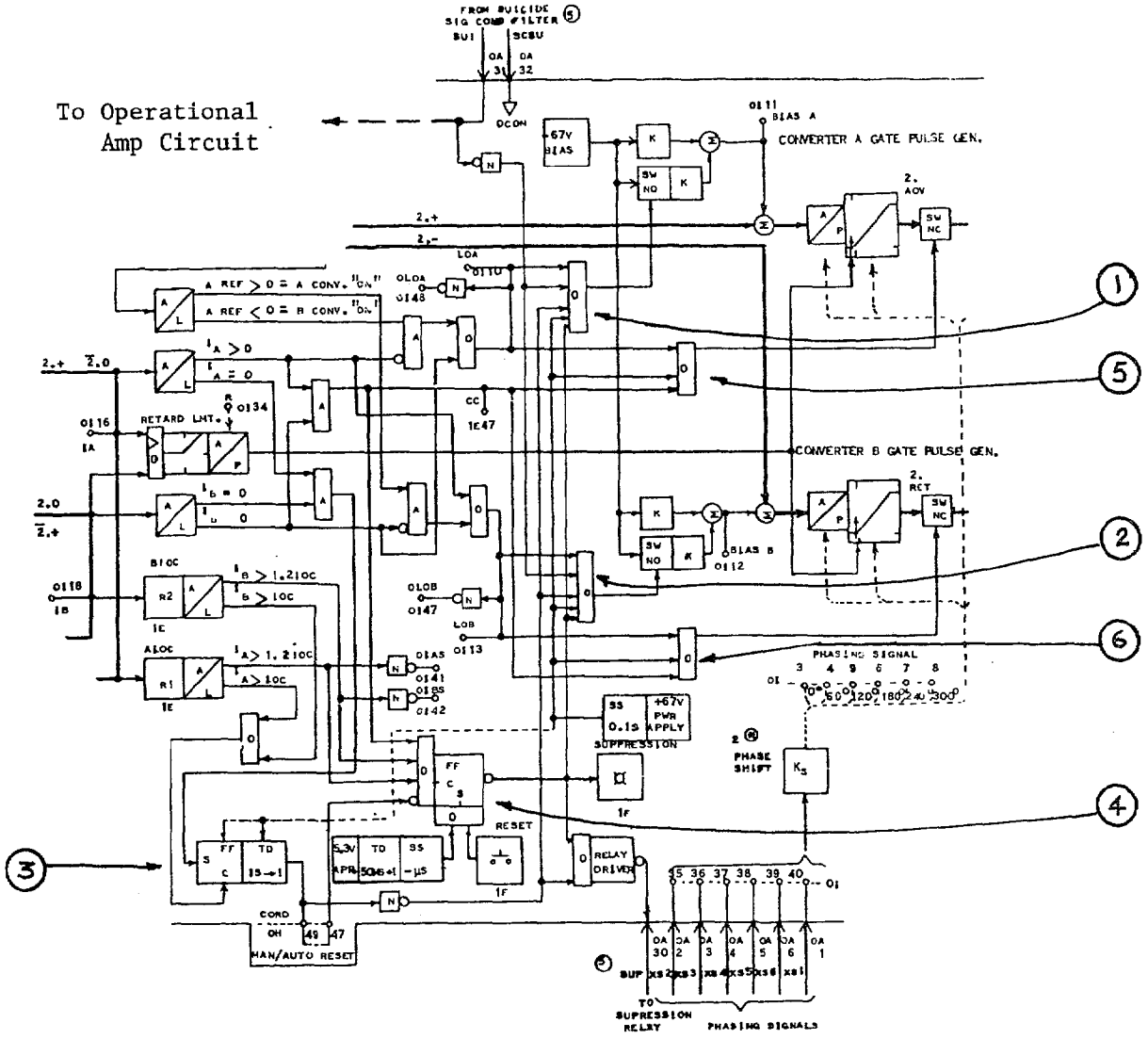


Figure 9

This portion of the firing circuit shows the various logic functions performed to provide the necessary protective features.

(1) and (2) - The outputs of these "OR" gates initiate a strong negative bias signal (-48 volts) to the A or B gate pulse generators, retarding pulses to retard limit.

REVERSING LOGIC AND OVERCURRENT PROTECTION (Cont'd)

The various inputs to the "OR" gates are as follows:

LOA (Lock out A) - This is a logic signal applied to (1) and generated as a function of Reference A, I_A, and I_B.

LOA is logic "1" if $I_B > 0$ OR if (Ref. A $<= 0$ and I_A is not > 0).

The second input to (1) is a suicide signal from the drive regulator retarding pulses to retard limit when the drive regulator is suicided. This signal is also applied to (2).

The third input to (1) is generated from the overcurrent logic which is discussed later. This signal is also applied to (2).

The fourth input to (1) is a 0.1 second pulse retarding pulses during application of 67V power. This signal is also applied to (2).

The fifth input to (1) is also generated from the overcurrent protection which is discussed later. Again, this signal is also applied to (2).

LOB (Lock Out B) - This is a logic signal applied to (2) and generated as a function of Ref. A, I_A and I_B.

LOB is logic "1" if $I_A > 0$ OR (Ref. A > 0 and I_B is not > 0).

(3) - This flip-flop is "set" on application of 67V power or when -

$$(I_A = 0 \text{ and } I_B = 0)$$

When an IOC (first level) overcurrent condition exists, the flip-flop is "cleared" and gives a logic "0" output. The clear signal is obtained when -

$$(I_A > \text{IOC or } I_B > \text{IOC})$$

The "0" output is inverted and applied to OR gates (1) and (2) to bias both A and B gate pulse generators to retard limit. It is also applied to a relay driver to operate the suppression relay and trip out the drive.

The flip-flop has a time delay of 0.5 second when going from "0" to "1" to allow time for the drive to trip out and prevent mal-function by the current going to zero and resetting the flip-flop before the drive contactor has opened.

(4) - This flip-flop applies a strong bias via OR gates (1) and (2) and trips out the drive via the suppression relay for fault conditions that must be manually reset.

The flip-flop is "set" by application of 5.3V power OR by the RESET pushbutton.

The flip-flop is "cleared" when ($I_A > 0$ and $I_B > 0$) circulating current fault.

OR

($I_A >$ 1.2 IOC)

OR

($I_B >$ 1.2 IOC)

} Second Level Overcurrent

OR

($I_A >$ IOC)

OR

($I_B >$ IOC)

} First level overcurrent if connected via the coordination card pins 47 and 49.

(5) - This OR gate shows that in addition to retarding pulses to retard limit, gate pulses are suppressed for the following conditions:

LOA - Lock out A

CC - Circulating Current (current in packages A & B)

67V Power Apply - Pulses are inhibited for 0.1 seconds during application of power.

(6) - Similarly, for B gate pulse generator, pulses are suppressed for the following conditions:

LOB - Lock out B
CC - Circulating Current
67V Power Apply

GATE PULSE GENERATOR:

Throughout the gate pulse generator description, reference is made to phasing signals at various phase angles. Refer to Figure 10 for definition of these angles. The figure shows the relationship between the phasing signals and the power bridge inputs. (Power transformer secondary).

0° is defined as the power bridge input Line 1 to neutral.

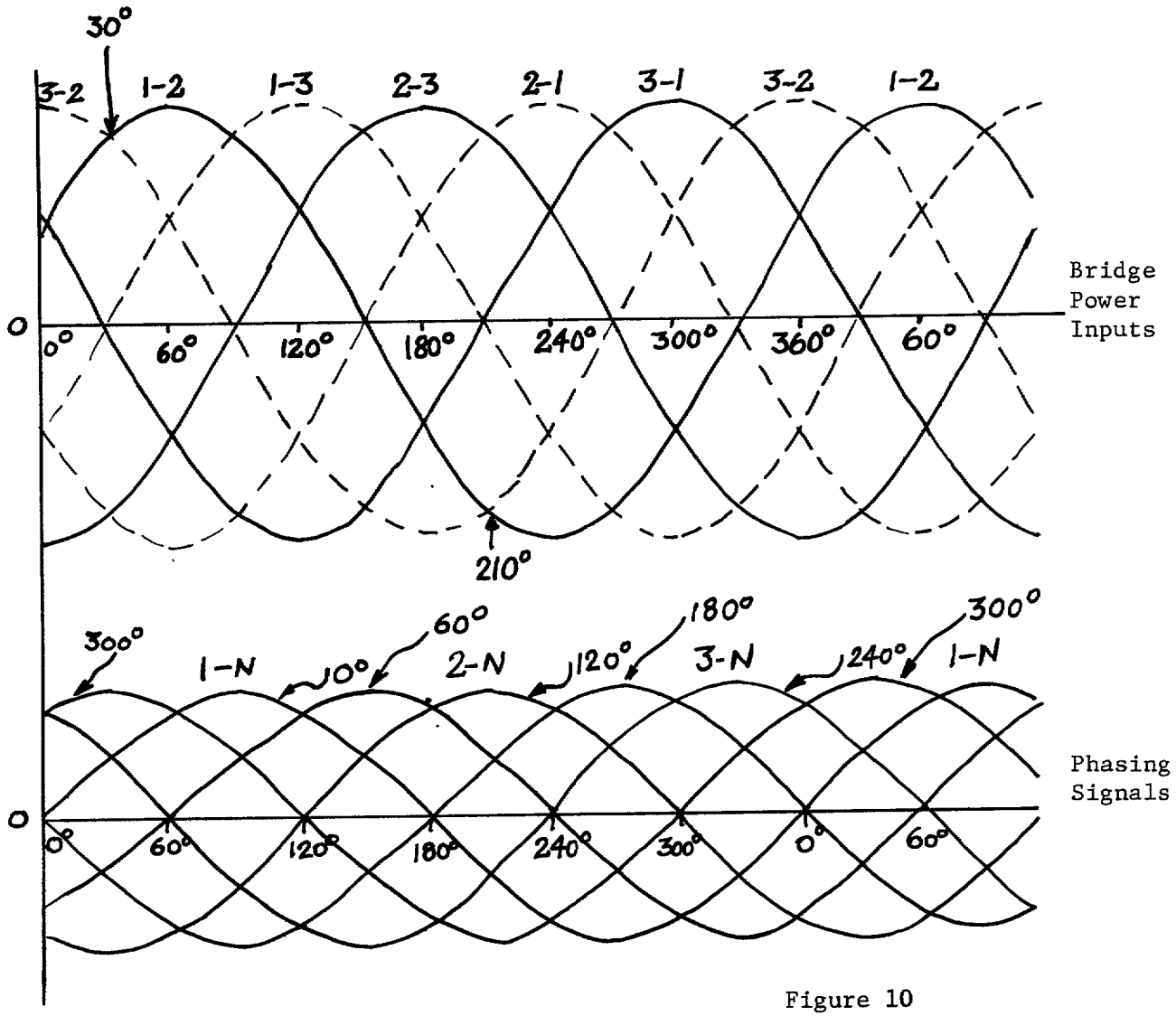


Figure 10

GATE PULSE GENERATOR (continued)

The phasing signals are derived from a phasing transformer which is a 50/60 cycle, three phase, 250VA device. The primary is normally connected in delta and the secondary in a six phase star. These six star windings are phasing reference waves. They are fed into a phase shift network card where they are conditioned for use in the firing circuit by means of RC filters. If the power transformer for the Siltrol is delta-delta connected, a thirty degree phase shift is introduced to the reference in the phase shift network. If the power transformer is delta wye connected, a zero shift is required in the phase shift network. However, the reference still requires filtering to avoid dips and spikes which are sometimes present on the a-c bus. Therefore, the filtering is designed to introduce a 60° phase shift. Because the 6 reference waves are 60° apart, the output of the phase shift network is connected to give the desired zero phase shift.

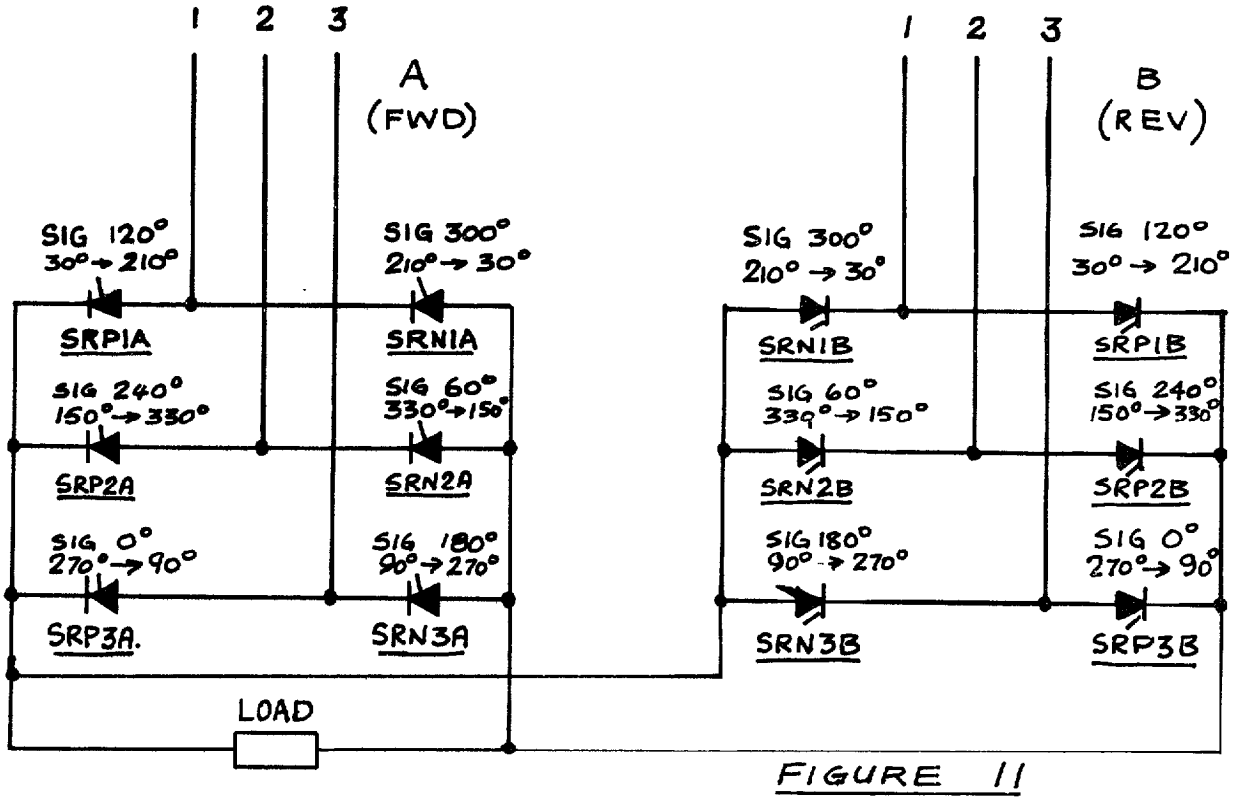


FIGURE 11

Consider the firing of cell SRP1A. Referring to figures 10 and 11, the allowable firing period for cell SRP1A is from 30° ⟶ 210°. Actually, to ensure good commutation it is desirable to limit full advance to around 36°. It is also necessary to limit maximum retard to around 185° but to advance the retard limit as a function of current, to ensure good commutation when inverting.

To fully understand how the advance and retard limit function, we will first consider the operation of the gate pulse generator card.

Gate Pulse Generator (Continued) -

Figure 12 is a block diagram showing functionally how a gate pulse generator card operates. There are 2 cards, one for each power bridge, A & B.

The various signal inputs to the card are as follows:

REF - For power bridge A, this is reference A, the output of the regulating amplifier, a DC voltage variable between ±25 volts.

BIAS - For power bridge A, this is Bias A, a DC level generated by the suppression and Bias card. It has two voltage states: -10V and -48V.

SIGNAL - This is the name assigned to the 6 sine wave references.

INVERTER LMT - These inputs are the 6 inverter limit inputs required to control the maximum retard angle and are discussed in detail later.

LOCKOUT - This input is derived from the reversing logic; its function having already been discussed.

The symbol for pulse generation for one cell only is shown in detail. The circuits for the other five are identical as indicated.

Considering P1 (cell SRP1A), it can be seen that "BIAS" and "REF" are summed with the 120° sine wave and the resultant if > 0 gives a logic "1". This is then applied to an OR gate with the inverter limit input. The output of the OR gate is applied to an AND gate with the advance limit signal (ADV LMT).

The output of the AND gate initiates a 50 μsec "0" pulse on P and "sets" a flip-flop, giving a "0" output on OGP. The flip-flop is "cleared" when the flip-flop of circuit P2 is "set" (120° later). Similarly, P2 is reset by P3 and P3 is reset by P1. The flip-flop is also reset whenever a lockout condition exists.

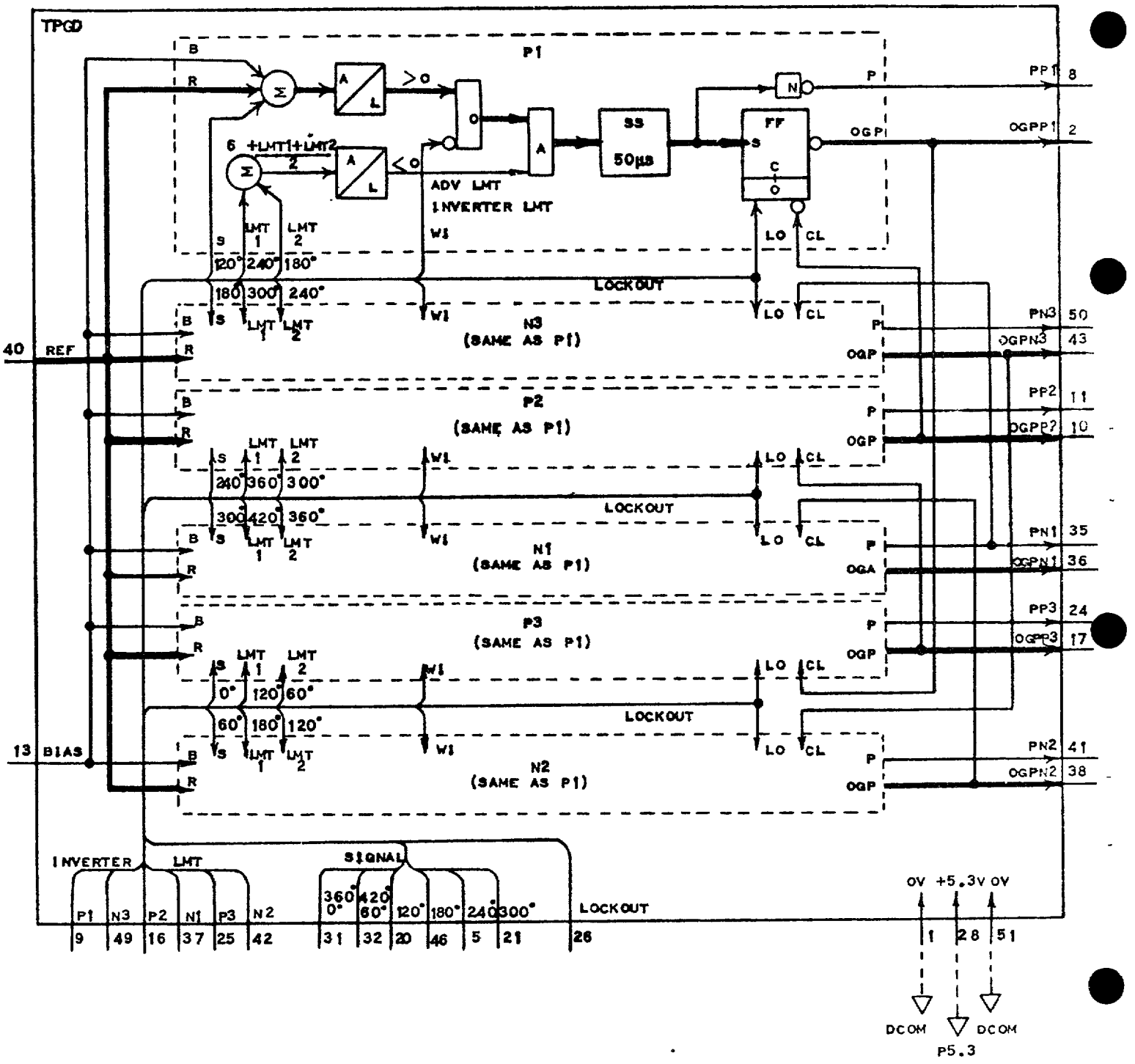
Figure 13 shows the generation of P and OGP for various values of REF.

The point at which pulses are generated during the allowed firing period (between advance limit and inverter limit) is determined by BIAS, REF, and for cell P1, the 120° sine wave. If BIAS is -10V and REF is +10V, then the cell will fire just as the 120° wave goes from a negative value to a positive value. On an inductive load, this will give 0V output.

If BIAS is -10V and REF 0V, pulses will be generated at approximately 137° retard, resulting in discontinuous current.

With -10V BIAS and 25V REF, a pulse will be generated at full advance or approximately 30°.

Note that except when BIAS and REF are equal and opposite pulses automatically tend to advance for reduced line voltage and retard for increased line voltage.



NOTE: ALL DEGREES SHOWN ARE UNDERSTOOD TO BE DEGREES LAGGING.

Figure 12

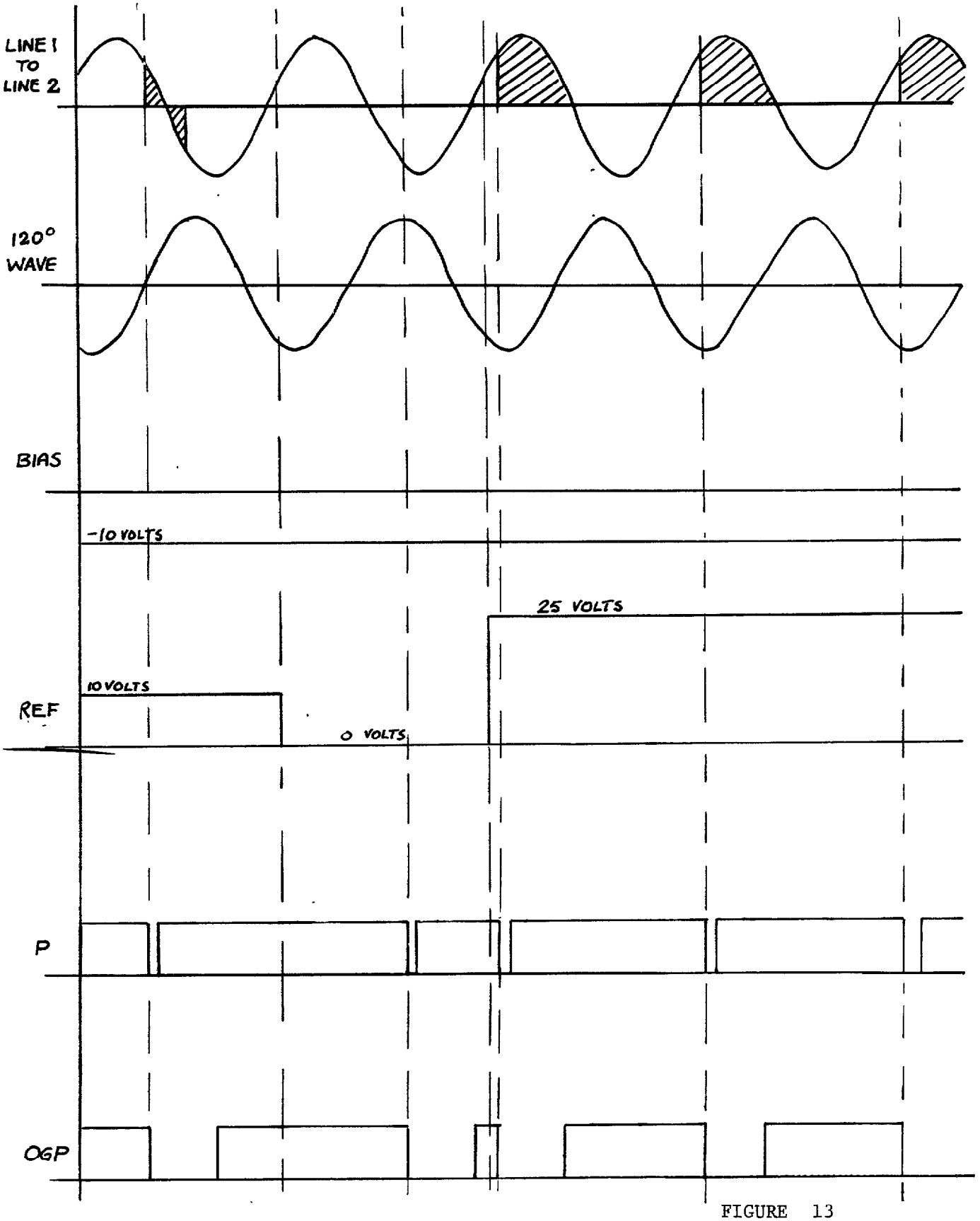

LINE 1
TO
LINE 2
120°
WAVE
BIAS
-10 VOLTS
25 VOLTS
10 VOLTS
REF
0 VOLTS
P
OGP

FIGURE 13

ADVANCE LIMIT

The advance limit is required to inhibit full advance to 36°. Referring to Figure 12, it can be seen that it is obtained by correctly weighting the 180°, and 240° waves and adding them, producing a 216° wave (see Figure 14). A logic "1" is produced whenever the 216° wave is negative (< 0); i.e., a logic "1" is produced for the period 36° → 216° and, hence, inhibiting pulse generation at any other phase angles.

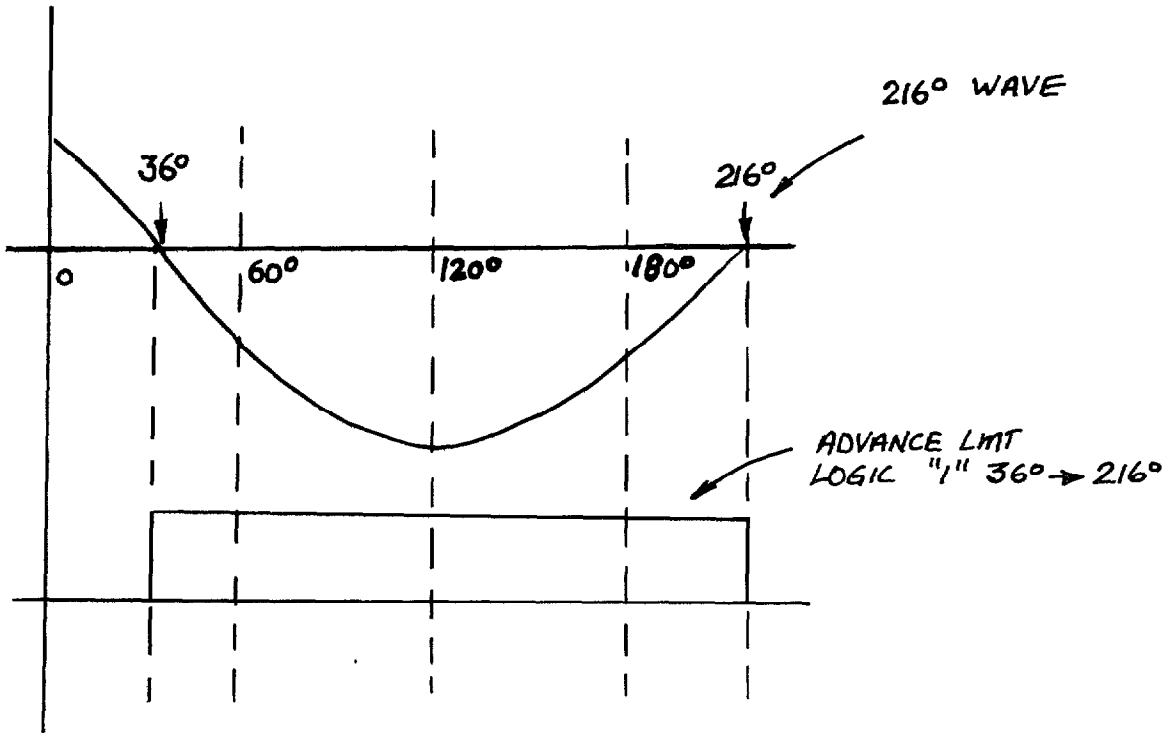


FIGURE 14

INVERTER LIMIT

Figure 15 is a symbol diagram showing functionally how the inverter limit card works. The symbol for P1 only is shown in detail.

The various inputs are as follows:

I_A & I_B - The current feedback signals are OR's as shown in Figure 15.

The OR symbol shows that if I_A or I_B are positive, then the output of the OR gate is an analog signal equal to the larger of I_A and I_B . Normally, I_A and I_B are not present simultaneously.

S1, S2 and S3 - These are the various sine waves required to produce the inverter limit function.

LOA, LOB - not used for Siltrol.

Figure 16 shows the various sine wave inputs and the resulting logic outputs. The 210° wave is obtained from the summation of the 180° and 240° waves. The 210° wave is then summed with the negative half of the 120° to give the third wave which, without Bias and I_A and I_B , inputs would be negative from approximately 330° to 210°. Referring to Figures 11 and 12, it can be seen that P1A and P1B are logic "0" from 210° to 330°.

The dotted lines "BIAS" and "I_A OR I_B " show how the retard limit angle advances when these d-c levels are introduced.

The dotted version of the third wave shows how the retard limit advances as a function of reduced line voltage.

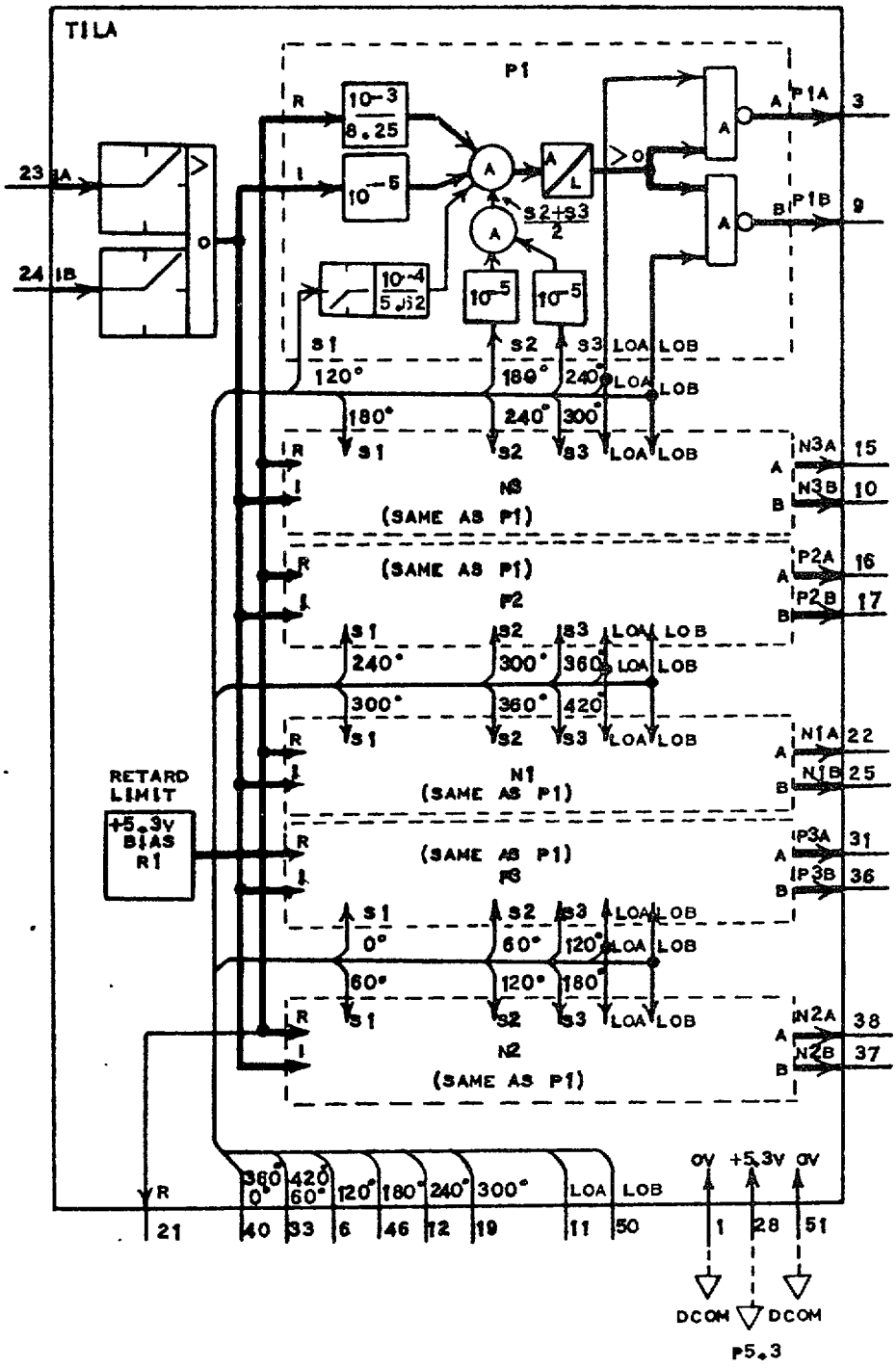

T1LA
P1
R
I
10⁻³ / 8.25
10⁻⁵
23 3A
24 3B
S1
120°
S2
180°
240°
S3
300°
LOA
LOB
P1A 3
P1B 9
N3
(SAME AS P1)
N3A 15
N3B 10
P2
P2A 16
P2B 17
360°
420°
N1
N1A 22
N1B 25
RETARD LIMIT
+5.3V BIAS R1
IP3
IP3A 31
IP3B 36
0°
60°
N2
N2A 38
N2B 37
21
40
33
6
46
12
19
11
50
0V
+5.3V
1
28
51
DCOM
P5.3

Figure 15

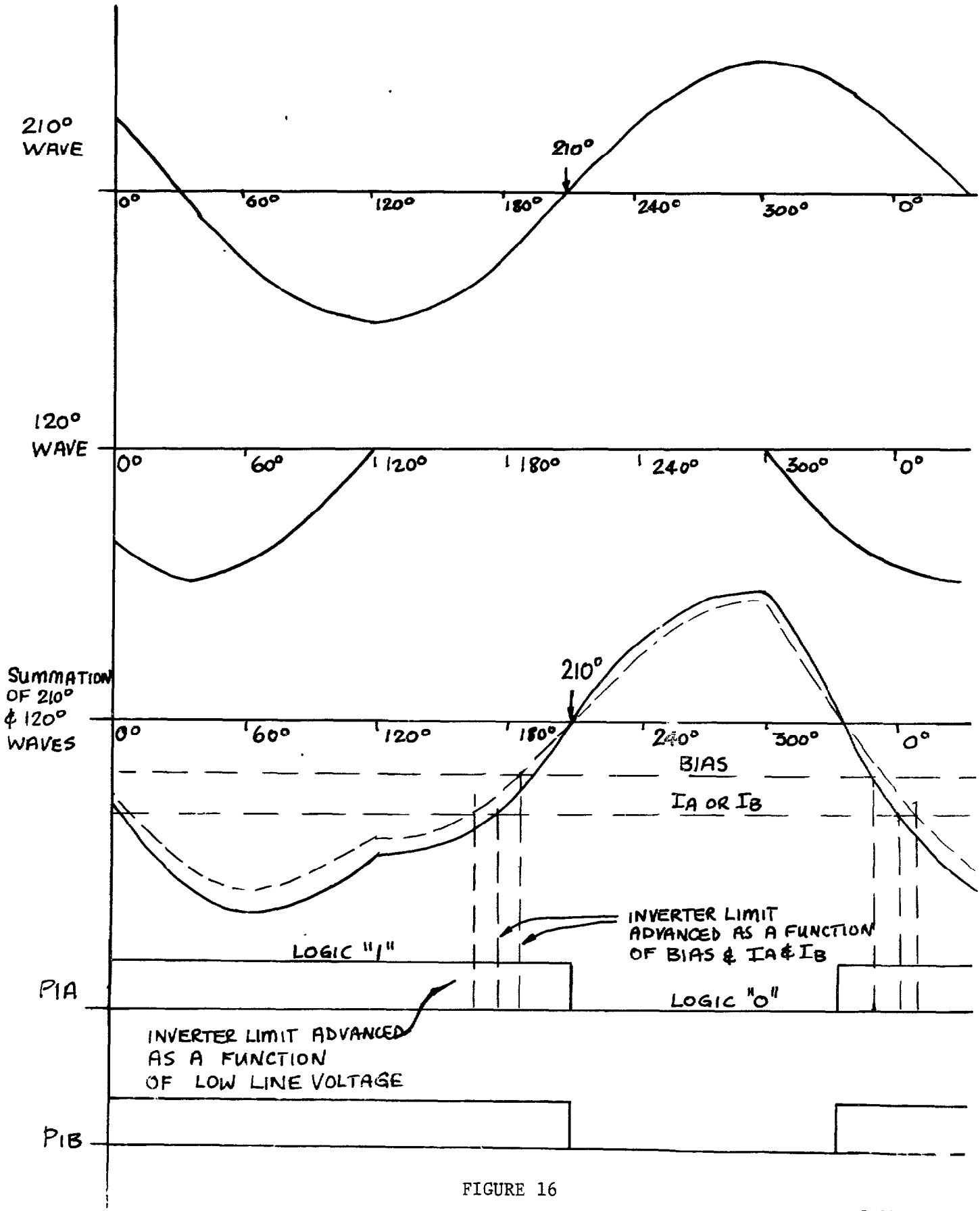

210° WAVE
210°
0°
60°
120°
180°
240°
300°
0°
120° WAVE
0°
60°
120°
180°
240°
300°
0°
SUMMATION OF 210° & 120° WAVES
210°
0°
60°
120°
180°
240°
300°
0°
BIAS
IA OR IB
INVERTER LIMIT ADVANCED AS A FUNCTION OF BIAS & IA & IB
LOGIC "1"
LOGIC "0"
PIA
INVERTER LIMIT ADVANCED AS A FUNCTION OF LOW LINE VOLTAGE
PIB

FIGURE 16

GATE PULSE AMPLIFIER

The gate pulse amplifier is designed to convert the low power microelectronic signal outputs of the gate pulse generator to relatively high power pulse trains, which are fed to pulse transformers (gating module). The pulse transformer outputs drive into the gates of the thyristors.

Figure 17 is a symbol showing functionally how the gate pulse amplifier operates.

The output OGP of the gate pulse generator is connected to terminal 2 (GLP1) of the gate pulse amplifier inverted in an OR gate (terminal 3 is not used) and then "ANDED" with the asymmetrical multi-vibrator output on P1 Pulse Amplifier. This gates the multi-vibrator output to the P1 Pulse Amp for the correct 120° period.

The output P of the gate pulse generator is connected to terminal 47 (PP1) of the gate pulse amplifier, and gated with the lockout signal in various ways as can be seen in Figure 17.

Assume that a lockout condition is present, in which case, there will be a "0" signal on the "FORCE 0" input to the asymmetrical multi-vibrator. This signal will force a "0" on the output of the vibrator inhibiting pulses.

If the lockout signal is removed, the vibrator starts oscillating ("0" for 40/μsec.; "1" for 20/μsec).

When a 50/μsec. pulse appears on PP1 (terminal 47) through the logic, a "FORCE 1" signal is generated, which forces a "1" on the output of the multi-vibrator, ensuring that the first pulse is of 50/μsec. duration, to ensure good firing.

The input on terminal 2 gates the pulse train through P1 Pulse Amplifier for the correct 120° period.

TP1 on pin 12 is a test point which reads the multi-vibrator output.

SYMBOL

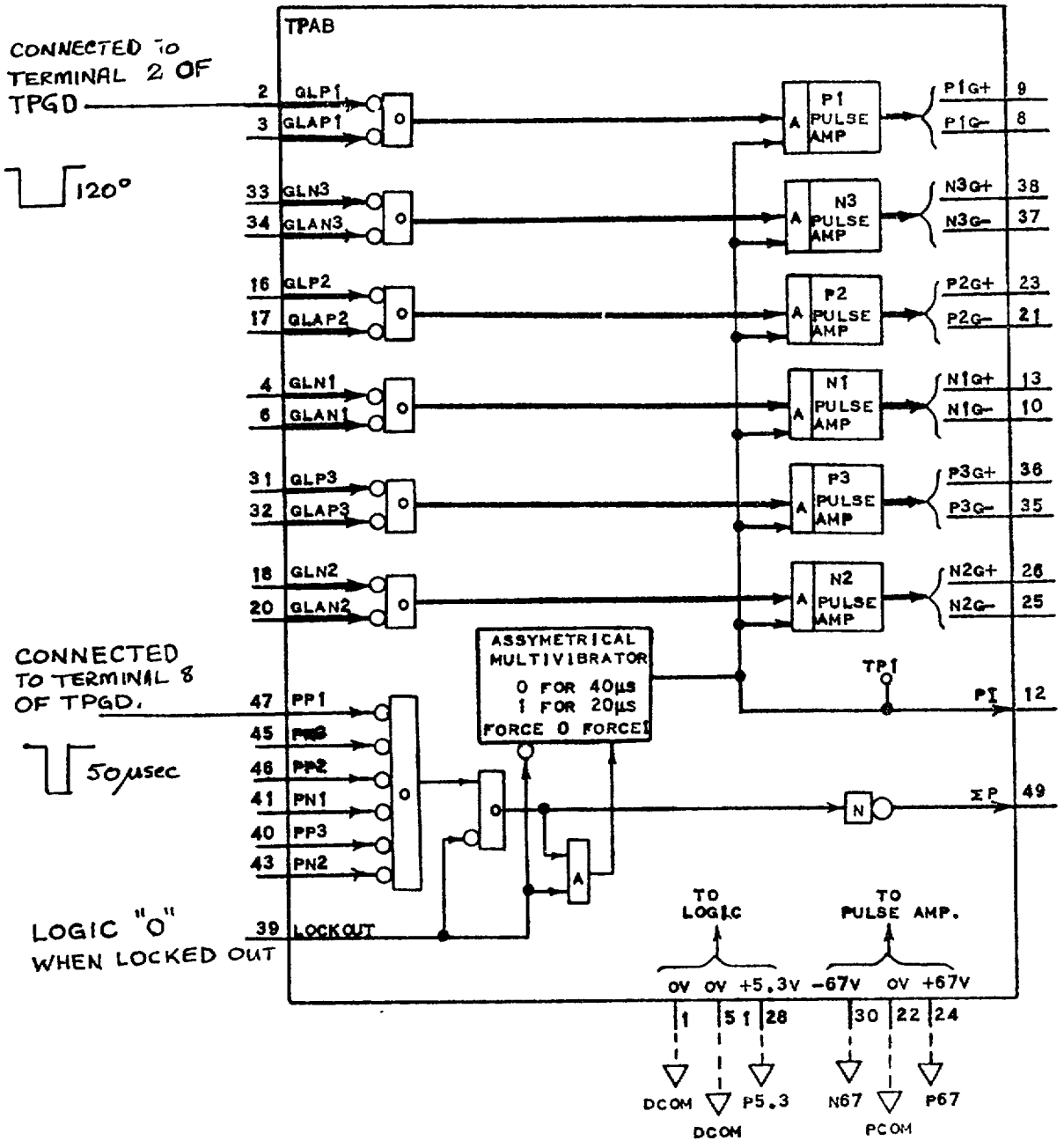


Figure 17

SILTROL I START-UP PROCEDURES

All Siltrol I units are completely factory tested and the line-ups are shipped as one unit. Therefore, field testing should be reduced to a simple check list and fine-tune with the actual drives. The purpose of these notes is to serve as a sequential guide for installation and checkout of the Siltrol equipments.

Precautions

First, the following precautionary advice is included to forewarn the tester against committing procedures which might tend to nullify important protective relationships that are designed into the system.

A. For those rectifiers fed from low voltage primary where the rectifier transformer is approximately 1:1 in turns ratio, DO NOT operate the rectifier directly from the primary source (bypassing the transformer). The transformer is designed with a specific value of reactance to limit available short-circuit current. Without this reactance the armature supply could be subject to loss of thyristors.

B. DO NOT megger control modules and circuits where solid state electronic devices are present, as they can be damaged easily.

When meggering rectifier power circuits, short all busses together to avoid impressing potential across rectifying devices unnecessarily. Hi-potting of rectifier power circuits is not considered advisable or necessary.

C. Use extreme care and caution when working with or around the rectifier power circuits and modules. They are by nature high capacity, low impedance paths, and a destructive arcing fault could be precipitated by careless procedure. For example connecting scope to d-c bus without proper probes is dangerous. Refer to oscilloscope techniques.

D. DO NOT operate the rectifier with Suppression circuit cards or a-c CT circuits opened. During inspection or trouble-shooting procedures, circuits may be systematically opened or isolated as logical maneuvers, but care must be taken not to nullify the Suppression function, or leave CT's open circuited.

E. To maintain the correct cooling capacity in the Siltrol equipment, it is imperative that none of the rear covers be removed prior to operating the equipment.

F. DO NOT operate the rectifier full-reversing on a regenerative load with the Reversing Logic or Suppression circuits disabled.

Oscilloscope Techniques

Observations of voltage and current waveforms in power rectifier circuits require extra care in selection and use of oscilloscope equipment. The make-up of the rectifier bridge circuit, whether grounded or not, produces large voltages to ground at nearly all points. In observing voltages or currents within the rectifier, differential signal circuits in the oscilloscope are used to reject these common mode voltages and to display the desired signal correctly.

In addition to more accurate observations, differential signal circuits are also safer to use since the oscilloscope chassis is grounded. The oscilliscope equipment should be provided with calibrated vertical deflection system to allow interpretation of observations. Since the oscilloscope equipment must accommodate the highest voltage in the rectifier, voltage probes are used to extend the voltage rating. These probes should be matched in rating and performance for use in differential observations. "Tektronic" Type 453 portable scope with suitable voltage and current probes is recommended to examine rectifier wave forms. For systems up to 600 volts use Type P6006-10X voltage probes. Type P6023 probes are often very useful to improve rejection of voltage signals to grounds for more accurate presentation of desired waveforms. To examine thyristor gate currents use Type P6021 current probe.

The sweep system should be calibrated in sweep speed, and should preferably be of a triggered type to allow reliable display of the signal. If waveforms are to be recorded on film, the sweep generator should also include a single sweep feature. Type 453 contains all those features.

The oscilloscope equipment suggested must be correctly adjusted to produce accurate results. First the pre-amplifier is adjusted for d-c balance (set AC-GND-DC switch to GND, set sweep mode switches to auto trig) by varying the step attenuator control until no trace of motion is seen as the variable vertical calibration control is moved from 20MV to 5MV. Both voltage probes must be adjusted for correct frequency compensation using the calibrator as a square wave standard and adjusting the a-c coarse compensation control in the termination box of the probe.

Voltage calibration of the probe and pre-amplifier is adjusted by the gain adjustment using the calibrator signal as a standard. The above operations are done with one signal circuit at a time. The scope is changed to display the difference between channel 1 and 2 by setting mode switch on ADD and inverting the channel 2 signal. Both probes are connected to the calibrator. Set calibrator on 1V. Turn trigger from normal to channel. Adjust gain control of channel 2 to obtain straight line with volts/div control set on 10MV per division for 10x probes. Next the pre-amplifier is changed to differential connection and both probes are connected to the calibrator. Adjust the d-c attenuator control and a-c compensation fine adjustment for the minimum signal display. In final adjustment, common mode rejection can be checked by connecting both probes to the same circuit point to be tested. The display should remain a straight and stationary line.

Siltrol I Checklist -- Full Reversing

1. Perform preliminary inspection as applicable to any new equipment. Check proper assembly and connection, both mechanical and electrical; loose, missing or damaged parts.

2. A "Siltrol Power Converter Design Variable Data Sheet" is supplied as part of the System Drive Elementary for each drive. Each System Drive Elementary also has a sheet showing the Siltrol Arm. Supply in block form with "application variable information." Using these sheets and the Siltrol Elem. check the following:

   A. Inspect Primary Breaker (Refer to GEH-2021C for AK type breakers)

   B. On Cards check:

      I Values of R12, R13, R14 and R15 on CCCA card, slot BOD.

      II All jumpers per drive elementary on CORD card, slot BOH.

3. Drive Magnetics and Drive Regulator

   A. Check out drive magnetics (line panel, relay panel, etc.) using system elementary. If drive has logic check out using system elementary.

   B. Ensure that Siltrol suicide circuit operates and is connected to Siltrol.

   C. Disable drive regulator.

4. Siltrol Tests

   A. Disconnect the power bridge from the rectifier transformer secondary.

   B. Connect resistive load to Siltrol output. (Suggest 10 ohms, 5KW).

   C. Select magnetics so that when suicide signal is lifted the M contactor closes and connects the load.

   D. Apply a suicide signal (i.e. suicide the Siltrol)

   E. Close a-c breaker and check the following:

      I Cooling blower motor should start and circulate air through the bridge from the front and then over the transformer. Motor rotation is correct when the fan runs with a high noise level and stops rapidly on removal of power. The blower air flow switch should close and operate relay BL.

      II Transformer overtemperature relay should energize.

III Verify presence of power with a multimeter at the following points:

+67V (+7V -4V) BOI	Pin 24	ACOM	BOI2
-67V (+7V -4V) BOI	Pin 30	ACOM	BOI2
+5.3V(+.5V-.5V) BOI	Pin 28	DCOM	BOI1

IV Ensure phase rotation is L_1, L_2, L_3, using a phase rotation meter or scope.

F. Connect a $\pm$ 15V d-c supply to REF 1 (Note: It may be convenient to use the drive regulator output). With zero signal check the presence of pulses at each thyristor gate using a current probe. Pulses should be present for package B only. Connect a 10K resistor across the operational amplifier, remove the suicide signal and swing REF 1 positive and negative and check that pulses advance smoothly and appear for one package at a time. Apply suicide signal and remove the 10K resistor.

G. Check the I_A and I_B logic operation and first and second overcurrent settings by injecting a milliamp signal into I_A (OI16) and I_B (OI18). Check the requisition elementary data sheet for milliamp settings for the overcurrent levels. If a suitable milliamp source is not available it may be necessary to remove the burden resistor R12, R13, R14, R15 on card CCCA and inject a suitable voltage signal to do the tests.

REPLACE THE BURDEN RESISTOR AFTER TEST.

H. Apply suicide signal and open Siltrol breaker. Reconnect the power bridge.

I. Reclose breaker and remove suicide signal. Check for zero output voltage. Note: The voltage regulator loop is now closed.

J. Vary REF 1 to $\pm$ 15 volts and observe d-c output voltage. The waveform produced should be a sawtooth with 60° spacing.

K. Set REF 1 to 7.5V and check that the d-c output is 50% of rated. VIA should be -7.5 volts.

L. Check operational amplifier output with a scope. The waveform should be a smooth 360 Hz ripple (300 Hz for 50 Hz power system) approximately 5V peak to peak in the continuous current region.

Unbalanced ripple or deviation from approximately 5V peak to peak indicates regulator instability.

M. Check that I_L feedback is correct in sense and magnitude.

N. Vary input from +VE to -VE and observe d-c output voltage with a scope for any irregularity.

O. Disconnect the Siltrol from the resistor and connect to the drive. The Siltrol tests are now complete except for a check of first and second level overcurrents with actual current. It is not recommended that excessive currents be circulated to check trip points, but actual current should be checked against I_A and I_B to check operation of the CT's.

Siltrol Checklist - Non-reversing

1- 4E. Perform these steps as for reversing drives.

4F. Connect a -15V DC variable supply to REF 1 (Note - It may be convenient to use the drive regulator circuit.) If the drive has a voltage regulator connect a 10K resistor across the operational amplifier. With zero signal check that pulses are present on all thyristor gates. Lift suicide and swing REF 1 negative and check that pulses advance smoothly. Apply suicide signal and remove 10K resistor.

G. Check I_A first and second overcurrent levels as for reversing drive.

H. Apply suicide signal and open the Siltrol breaker. Reconnect the power bridge.

I. Reclose breaker and remove suicide signal. Check for zero output volts and current. Note: If the drive has a Siltrol voltage regulator the loop is now closed.

J. Vary reference from zero to -15V and observe d-c output voltage. The waveform produced should be a saw tooth with 60° spacing. The waveform should remain evenly balanced in amplitude and spacing.

K. If drive has voltage regulator set reference to -7.5V and check that the d-c output voltage is 50% of rated. VIA output should be 7.5 volts.

L. If the drive has a voltage regulator the operational amplifier output waveform should be a smooth 360 Hz ripple (300 Hz for 50 Hz power system) approximately 5V peak to peak in the continuous current region.

Unbalanced ripple or deviation from approximately 5V peak to peak indicates regulator instability.

M. Check that the I_L feedback is correct in sense and magnitude.

N. Disconnect the Siltrol from the resistor and connect to the drive. The Siltrol tests are now complete except for a check of first and second level overcurrents with actual current. It is not recommended that excessive current be circulated to check trip points, but actual current should be checked against I_A to check operation of the CT's.

SECTION III TROUBLESHOOTING TECHNIQUES

In the event of trouble with Siltrol equipment the most important consideration is normally to get the drive back on line as soon as possible. It is therefore important that the troubleshooter have a good understanding of the functional operation to quickly localize the trouble.

It is often very helpful to determine what the process conditions were immediately before the failure, and to have available the Maintenance Log Book, to help determine the cause of the trouble.

If the trouble is localized to a printed circuit card it should be replaced with a spare and the Siltrol rechecked.

The use of a good oscilloscope is required to troubleshoot this equipment - Refer to the instructions on the use of oscilloscopes in Section 2 - "Siltrol I Start-Up Procedures."

DETAILED TROUBLESHOOTING NOTES

Although all Siltrol I units are completely factory tested detailed tuneup instructions are given here to help troubleshoot the equipment in the event of unforseen problems.

A. Firing Circuit -- Full Reversing

1. If the firing circuit is giving trouble, then, to avoid damage to the cells, disconnect the power bridge from the rectifier transformer secondary. This can be done below the thyristor power bridge in the vicinity of the ACCT's. DO NOT DISCONNECT AC LINE FILTER FROM TRANSFORMER SECONDARY.

2. Check TLF cards

   Refer to the following table for correct card.

Hz	Trans. Conn.	Correct Card
50	Δ-Y	TLFB
50	Δ-Δ	TLFD
60	Δ-Y	TLFA
60	Δ-Δ	TLFC

3, Remove coordination card (BOH) and insert dummy "open loop" coordination card if available. If not available open voltage regulator loop by removing a jumper on the coordination card.

4. Check the following cards to ensure that the correct form has been put into the page.

   a) AOAF - Slot BOG (Small and Medium HP); BOH (Large HP)

      Full Reversing uses AOAF2
      Non Reversing uses AOF1

   b) Gating Module

      Full Reversing uses 6TGD ___ cards.
      Non Reversing uses 3TGD ___ cards and 3 component boards with resistors (68A99701 ___).

   The type card used is a function of a-c voltage to the power bridge.

Voltage (Trans Secondary)	Use Card	Component Card Non-Reversing
460 to 505 VAC	TGDA	68A9970DA1 (180K)
350 to 380 VAC	TGDB	68A9970DB1 (120K)
230 to 290 VAC	TGDC	68A9970DC1 (82K)
230 to 505 VAC	TGDD	

5. Check phase rotation of input a-c power. Ensure phase rotation is:

1.	L1 to L2	X1 to X2 (R1 to R2)	H12 to H22
2.	L2 to L3	X2 to X3 (R2 to R3)	H22 to H32
3.	L3 to L1	X3 to X1 (R3 to R1)	H32 to H12

6. Line Filter Reference Phasing: By means of an oscilloscope, check phasing of the reference transformer and line filters.

   a) Set up scope so that 1cm equals 30° (i.e. make one half cycle of the reference sine wave equal six divisions.)

   b) Use external sync connected to BOI3 (0°); connect scope ground terminal to BOI1 (DCOM).

   c) Use single ended input, Chan. A with amplitude at 50V/cm; put input on BOI3 (0°).

d) Use Chan. B with amplitude at 50V/cm put input on BOI4 (60°). Chan. B should lag A by 60°. Move Chan. B to BOI9 (120°) and check B lags A by 120°. Similarly for BOI6 (180°), BOI7 (240°), BOI8 (300°).

e) Move Chan. B to L1. For $\Delta-\Delta$ power transformer connection Chan. B should be in phase with Chan. A; for Δ - Y connection Chan. B should lead Chan A by 30°.

7. Open Loop Test from Process Regulator Input to Thyristor Gate:

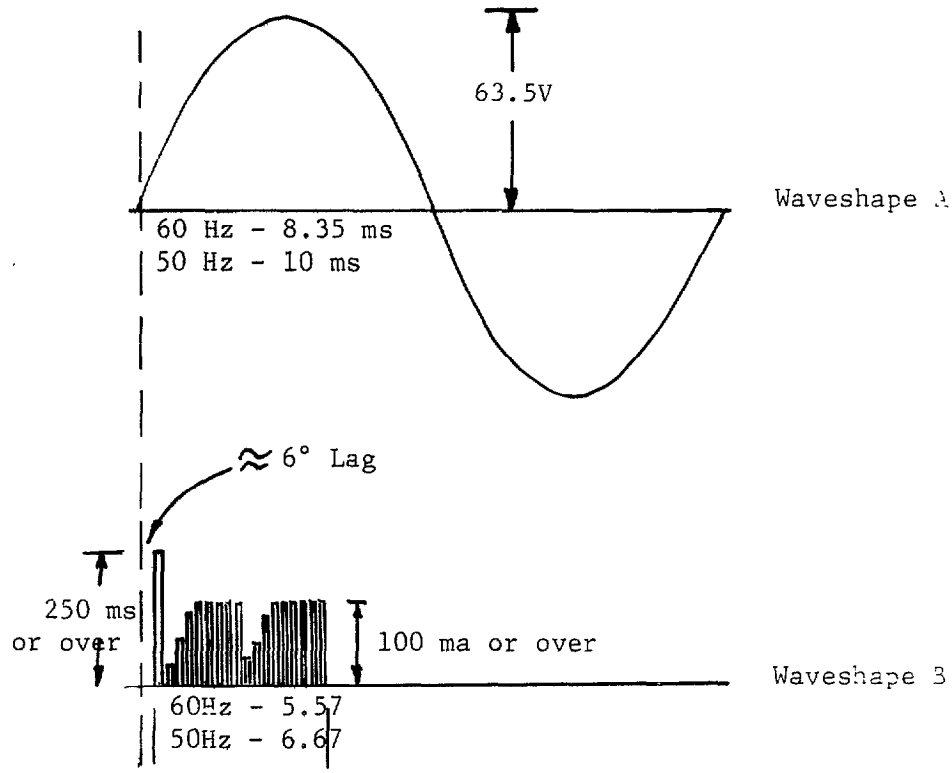
a) Ensure that the process regulator and VIA are disconnected at TB1

b) Connect +25V d-c supply to BOI21 (REF 1) and pick up suicide relay.

c) Use external trigger on the oscilloscope and connect to BOI3 (0°). Use both channels A and B and connect per following chart. If available use a current probe on Channel B.

Channel A	Channel B	Waveshape A	Waveshape B
BOI9 (120°)	PIAG (W)	63.5±7V pk sine wave	Pulse train originating at 6° lag of Waveshape A
BOI7 (240°)	P2AG (W)		
BOI3 (0°)	P3AG (W)		
BOI8 (300°)	N1AG (W)		
BOI4 (60°)	N2AG (W)		
BOI6 (180°)	N3AG (W)		

See TRACE A



TRACE A

d) Connect multimeter to regulating amplifier output. BOI26 for Small HP or Medium HP; BOJ26 for Large HP.

NOTE: For Type 1 voltage regulator connect suitable resistor across the regulating amplifier feedback to obtain finite control of the output.

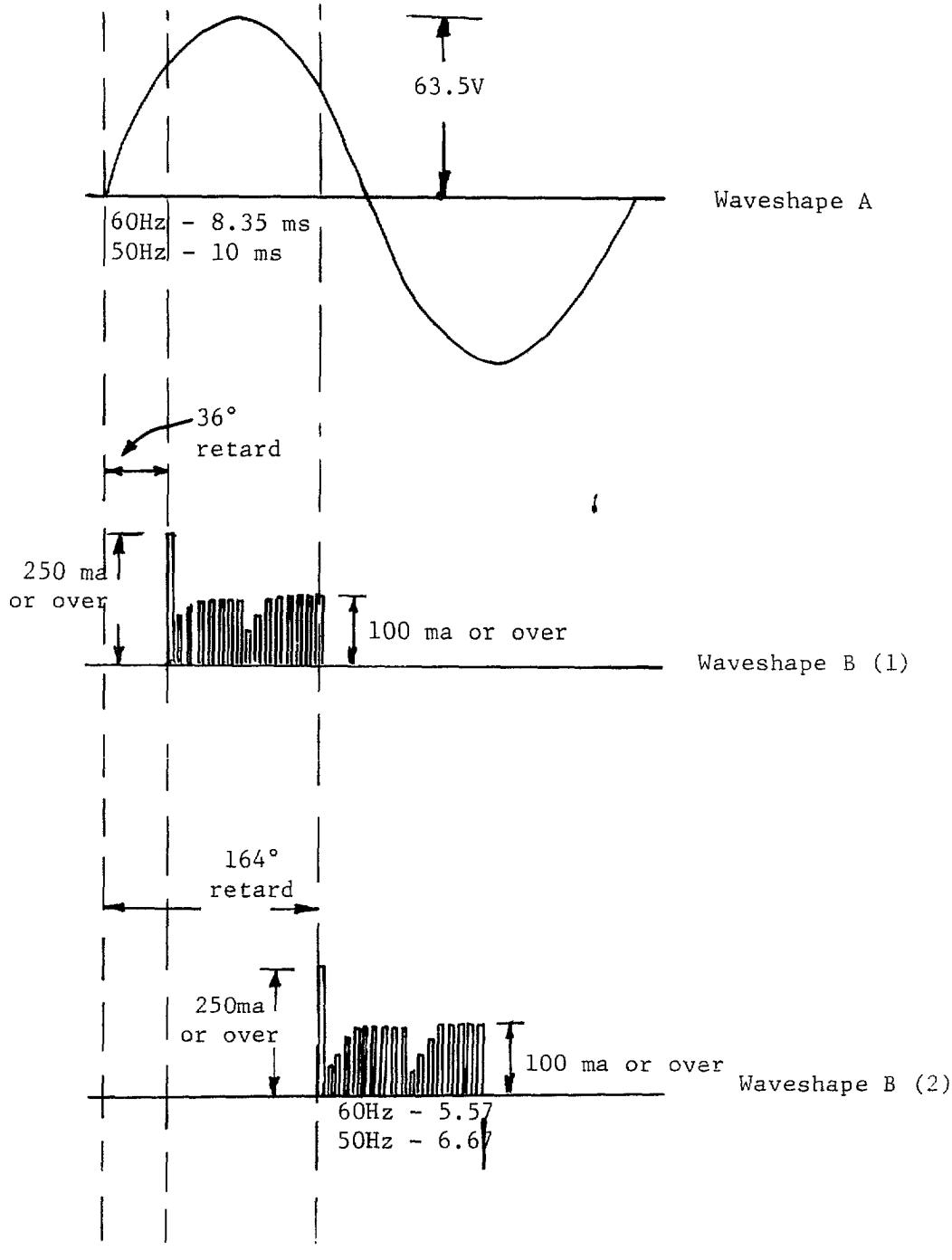
Vary the input source so that the regulating amplifier output varies from 0V to 25V DC. Observe the pulse train on Channel B and ensure that it retards smoothly in response to the input voltage change.

Check the maximum and minimum retard angle by observing the waveshapes for the following conditions:

BOI26	Chan. A	Chan. B	Waveshape A	Waveshape B
25V	BOI3 (0°)	P1AG (W)	63.5V ±7V pk. sinewave	(1) Pulse train at 36° ± 4° retard
0V	BOI3 (0°)	P1AG (W)	"	*(2) Pulse train at 164° ± 10° retard
25V	BOI9 (120°)	P2AG (W)	"	(1)
0V	BOI9 (120°)	P2AG (W)	"	(2)
25V	BOI7 (240°)	P3AG (W)	"	(1)
0V	BOI7 (240°)	P3AG (W)	"	(2)
25V	BOI6 (180°)	N1AG (W)	"	(1)
0V	BOI6 (180°)	N1AG (W)	"	(2)
25V	BOI8 (300°)	N2AG (W)	"	(1)
0V	BOI8 (300°)	N2AG (W)	"	(2)
25V	BOI4 (60°)	N3AG (W)	"	(1)
0V	BOI4 (60°)	N3AG (W)	"	(2)

See TRACE B

*The pulse train retard angles should match each other to within 2°. Absolute retard angle may vary Siltrol to Siltrol.


63.5V
Waveshape A
60Hz - 8.35 ms
50Hz - 10 ms
36°
retard
250 ma
or over
100 ma or over
Waveshape B (1)
164°
retard
250ma
or over
100 ma or over
Waveshape B (2)
60Hz - 5.57
50Hz - 6.67

TRACE B

e) Adjust variable supply to -25V d-c. Use both channel A and B and connect per following chart. If available use a current probe on channel B.

Channel A	Channel B	Waveshape A	Waveshape B
BOI9 (120°)	P1BG (W)	63.5 ± 7V pk. sinewave	Pulse train originating at 6° lag of Waveshape A
BOI7 (240°)	P2BG (W)		
BOI3 (0°)	P3BG (W)		
BOI8 (300°)	N1BG (W)		
BOI4 (600°)	N2BG (W)		
BOI6 (180°)	N3BG (W)		

See TRACE A

Vary the input source so that the regulating amplifier output varies from 0V to -25V d-c. Observe the pulse train on Channel B and ensure that it retards smoothly in response to the input voltage change.

Check the maximum and minimum retard angle by observing the waveshapes for the following conditions.

BOI26	Chan. A	Chan. B	Waveshape A	Waveshape B
-25V	BOI3 (0°)	P1BG (W)	63.5V ±7V pk sinewave	(1) Pulse train at 36° ± 4° retard
0V	BOI3 (0°)	P1BG (W)	"	*(2) Pulse train at 164° ± 10° retard
-25V	BOI9 (120°)	P2BG (W)	"	
0V	BOI9 (120°)	P2BG (W)	"	
-25V	BOI7 (240°)	P3BG (W)	"	
0V	BOI7 (240°)	P3BG (W)	"	See TRACE B
-25V	BOI6 (180°)	N1BG (W)	"	
0V	BOI6 (180°)	N1BG (W)	"	
-25V	BOI8 (300°)	N2BG (W)	"	
0V	BOI8 (300°)	N2BG (W)	"	
-25V	BOI4 (60°)	N3BG (W)	"	
0V	BOI4 (60°)	N3BG (W)	"	

* The pulse train retard angles should match each other to within 2°. Absolute retard angle may vary Siltrol to Siltrol.

8. Current Feedback I_A, I_B, I_L Suppression Bias, Lockout.

a) Connect a variable d-c source to BOI16 (I_A) and BOI50 (ACOM) and monitor it with a multimeter. Connect Channel A of the scope to BOI11 (BIAS A) and Channel B to BOI49 (OLOB).

b) Slowly vary the variable supply voltage as shown below. The monitor should act as follows: if coordination card is connected for AUTO RESET.

Var. Supply	BIAS A	OLOB	Light DSI
0	-48V	+5.3V	OFF
+.3V ±.1V	- 9.75	0V	OFF
* IOCMa	-48V	0V	OFF
1.2 IOCMa	-48V	0	ON
0	-48V	+5.3V	ON

Push reset PB to put light DSI off.

If coordination card is connected for Man. Reset.

0	-48V	+5.3V	OFF
+.3V ±.1V	- 9.75V	0V	OFF
* IOCMa	-48V	0V	ON
0	-48V	+5.3V	ON

Push reset button to put light DSI off.

0	-48V	+5.3V	OFF
1.2 OICMa	-48V	0V	ON
0	-48V	5.3V	ON

*See system elementary for value of IOCMa.

c) Set variable supply to feedback current indicated on system elementary and check that BOI20 (I_L) equals 15V. For fine adjustment adjust R16 on BOD. (Small and Medium HP); BOE (Large HP)

d) Connect the variable supply to BOI18 (I_B) and BOI50 (ACOM) (Small and Medium HP); BOJ18 (I_B) (Large HP) and monitor it with a multimeter. Connect Channel A to BIAS B and Channel B to OLOA.

Connect approximately 5 volts to REF 1 or REF 2 (It may be possible to use output of drive regulator). This removes the lockout signal from A package and locks out B package.

e) Slowly vary the variable supply voltage as shown below. The monitors should act as follows if the coordination card is connected for AUTO RESET.

Var. Supply (I_B)	BIAS B	OLOA	Light DSI
0	-48V	5.3V	OFF
+.3V ±.1V	- 9.75V	0V	OFF
* IOC	-48V	0V	OFF
1.2 IOC	-48V	0V	ON
0	-48V	+5.3V	ON

Push reset PB to put light DSI off.

If coordination card is connected for Manual Reset

0	-48V	+5.3V	OFF
+.3V ±.1V	- 9.75V	0V	OFF
* IOC	-48V	0V	ON
0	-48V	+5.3V	ON

Push reset PB to put light DSI off.

0	-48V	+5.3V	OFF
1.2 IOC	-48V	0V	ON
0	-48V	5.3V	ON

9. Inverter Limit

a) Connect BOI10 (LOA) to BOI51 (DCOM) to disable LOA.

b) Connect a variable d-c supply to REF 1 and monitor with a scope as below:

REF 1	Chan. A	Chan. B	Waveshape A	Waveshape B
-15 volts	BOI6 (180°)	P1AG (W)	63.5V ± 7V pk Sinewave	Pulse train at 5° nominal retard
"	BOI8 (300°)	P2AG (W)	"	"
"	BOI4 (60°)	P3AG (W)	"	"
"	BOI3 (0°)	N1AG (W)	"	"
"	BOI9 (120°)	N2AG (W)	"	"
"	BOI7 (240°)	N3AG (W)	"	"

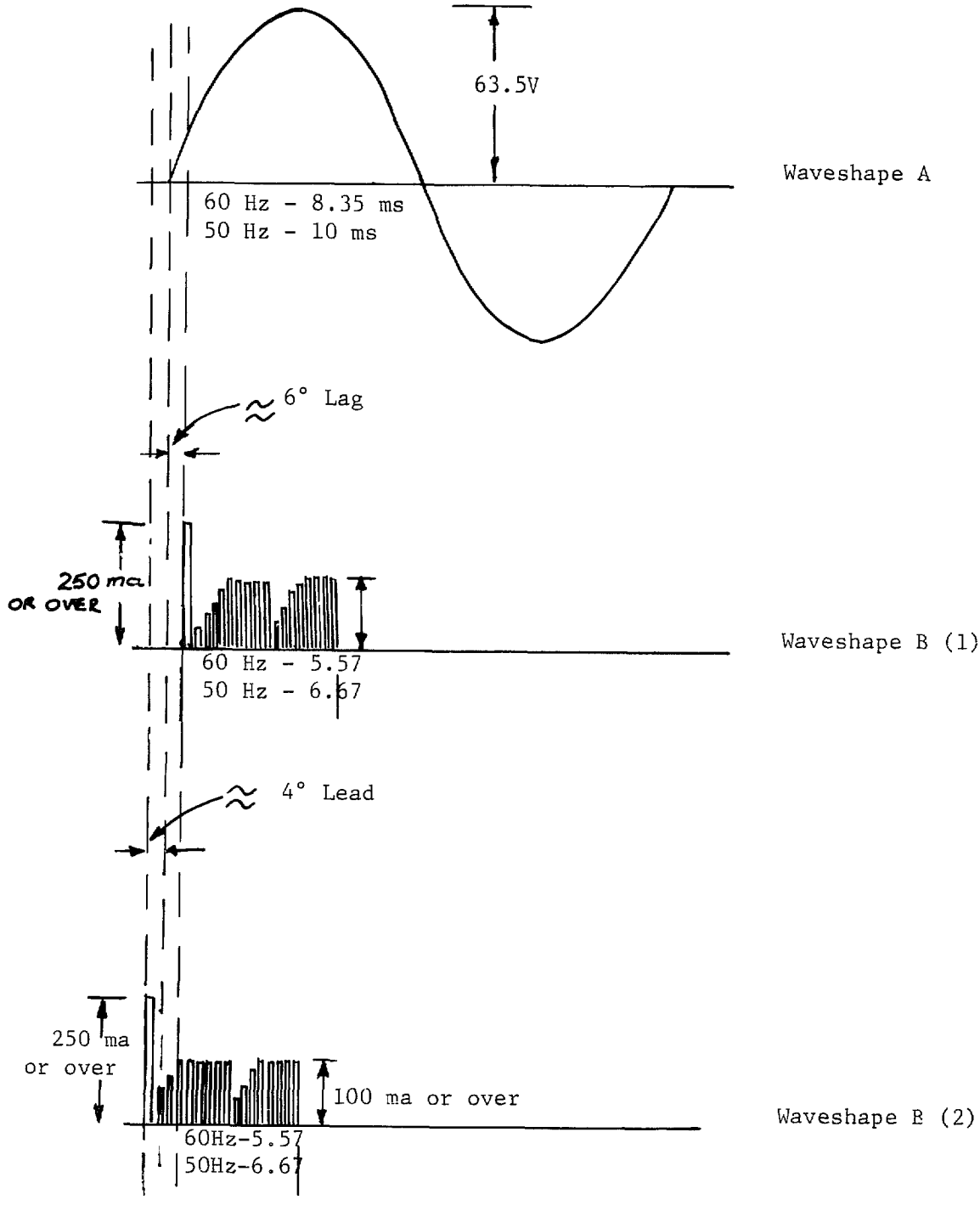
c) Connect signal equal to approximately 90% IOC to BOI16 (Ia) the pulse train should advance to 4° advance ± 2°. See TRACE C. Waveshape B (1) and B (2).

d) Similarly for B package. Connect BOI13 (LOB) to BOI51 (DCOM)

e) Connect monitors as shown below:

REF 1	Chan. A	Chan. B	Waveshape A	Waveshape B
+15 volts	BOI35 (180°)	P1BG (W)	63.5V ± 7V pk	Pulse train at
"	BOI37 (300°)	P2BG (W)	Sinewave	5° nominal retard
"	BOI39 (60°)	P3BG (W)	"	"
"	BOI38 (0°)	N1BG (W)	"	"
"	BOI40 (120°)	N2BG (W)	"	"
"	BOI36 (240°)	N3BG (W)	"	"

f) Connect a signal equal to approximately 90% IOC to BOI18 (Ib) the pulse train should advance to 4° ± 2° advance. See TRACE C


63.5V
Waveshape A
60 Hz - 8.35 ms
50 Hz - 10 ms
6° Lag
250 ma
OR OVER
Waveshape B (1)
60 Hz - 5.57
50 Hz - 6.67
4° Lead
250 ma
or over
100 ma or over
Waveshape B (2)
60Hz-5.57
50Hz-6.67

TRACE C

10. Bridge Power Output Tests - Resistive Load - Open Voltage Loop

a) Ensure all power is off and connect the power bridge to the transformer secondary. Remove gate pulse amplifier cards B1B and B1H.

b) Select magnetics etc., so that M contactor is picked up and load is connected.

c) Reapply power and check that voltage and current meters are at zero and all neon lamps 1LP1, 2, 3, and 1LN1, 2, 3 are burning.

d) Remove power and reinsert card B1B (TPAB).

e) Connect the scope across P and X in differential mode and ground the case of the scope.

f) Reapply power and vary the reference (REF1) so that the regulating amplifier output varies from 0-25V.

The d-c output should vary from zero to 1.3X transformer secondary RMS volts. The ripple produced should have a saw-tooth appearance with 60° spacing. The waves should remain evenly balanced in amplitude and spacing.

g) Check operation of lockout circuit by observing point BOI49 (CLOB). With a slightly positive reference BOI49 (CLOB) should go to OV.

h) Check calibration of current feedback by comparing actual current in the load against voltage produced at BOI20 (I_L). For calibration adjust R16 on CCCB, slot BOD.

i) Remove power; insert B1H (TPAB) and remove B1B (TPAB).

j) Reapply power and vary the reference (REF1) so that the regulating amplifier varies from 0 to -25V and repeat preceeding checks for package B.

11. a) Remove power and reinsert B1B (TPAB)

b) Reapply power and vary input so that regulating amplifier swings from 0 to $\pm$25V. Check the voltage and current varies in response to input switch from one package to the other through zero.

c) Remove power.

12. Close voltage regulator loop.

    a) Reconnect VIA output.

    b) Close voltage regulator by removing "open loop" coordination card (BOH) and inserting drive coordination card. (If "open loop" card was not available replace jumper removed for open loop test).

    c) Reapply power and check for zero output voltage.

    d) Increase reference to +7.5V and check that output voltage is 50% of rated and that VIA output is -7.5V.

    Reverse reference to -7.5V and check that output voltage is -50% of rated and that VIA output is 7.5V.

    If adjustment of VIA output is required adjust 1RH (RBK. ADJ. POT)

    e) Connect Channel A of the scope to BOI14 (VIA) and Channel B to BOI26 (OA). Swing the reference positive and negative. VIA should have a saw tooth waveshape and OA output should have smooth 360 Hz ripple (300 Hz for 50 Hz systems) approximately 5 volts peak to peak in the continuous current region.

B. Firing Circuit -- Non-reversing

1. If the firing circuit is giving trouble then to avoid damage to the cells disconnect the power bridge from the rectifier transformer secondary. This can be done below the thyristor power bridge in the vicinity of the ACCT's. DO NOT DISCONNECT AC LINE FILTER FROM TRANSFORMER SECONDARY.

2. Check TLF cards

   Refer to the following table for correct card:

Hz	Trans. Conn.	Correct Card
50	Δ – Y	TLFB
50	Δ – Δ	TLFD
60	Δ – Y	TLFA
60	Δ – Δ	TLFC

3. Remove coordination card (BOH) and insert dummy "open loop" coordination card if available. If not available open voltage regulator loop by removing a jumper on the coordination card.

4. Check the following cards to ensure that the correct form has been put into the page.

   a) AOAF - Slot BOG

      Non Reversing uses AOF1

   b) Gating Module

      Non Reversing uses 3TGD ___ cards and 3 component boards with resistors (68A99701 _).

The type card used is a function of a-c voltage to the power bridge.

Voltage (Trans Secondary)	Use Card	Component Card Non Reversing
460 to 508 VAC	TGDA	68A99701DA1 (180K)
350 to 380 VAC	TGDB	DB1 (120K)
230 to 290 VAC	TGDC	DC1 (82K)
230 to 505 V AC	TGDD	

5. Check phase rotation of input a-c power. Ensure phase rotation is:

1.	L1 to L2	X1 to X2 (R1 to R2)	H12 to H22
2.	L2 to L3	X2 to X3 (R2 to R3)	H22 to H32
3.	L3 to L1	X3 to X1 (R3 to R1)	H32 to H12

6. Line Filter Reference Phasing: By means of an oscilloscope, check phasing of the reference transformer and line filters.

   a) Set up scope so that 1cm equals 30° (i.e. make one half cycle of the reference sinewave equal six divisions.)

   b) Use external sync connected to BOI3 (0°); connect scope ground terminal to BOI1 (DCOM).

   c) Use single ended input, Chan. A with amplitude at 50V/cm; put input on BOI3 (0°).

   d) Use Chan. B with amplitude at 50V/cm put input on BOI4 (60°). Chan. B should lag A by 60°. Move Chan. B to BOI9 (120°) and check B lags A by 120°. Similarly for BOI6 (180°), BOI7 (240°), BOI8 (300°).

   e) Move Chan. B to L1. For Δ−Δ power transformer connection Chan. B should be in phase with Chan. A; for Δ - Y connection Chan. B should lead Chan. A by 30°.

7. Open Loop Test From Process Regulator Input to Thyristor Gate:

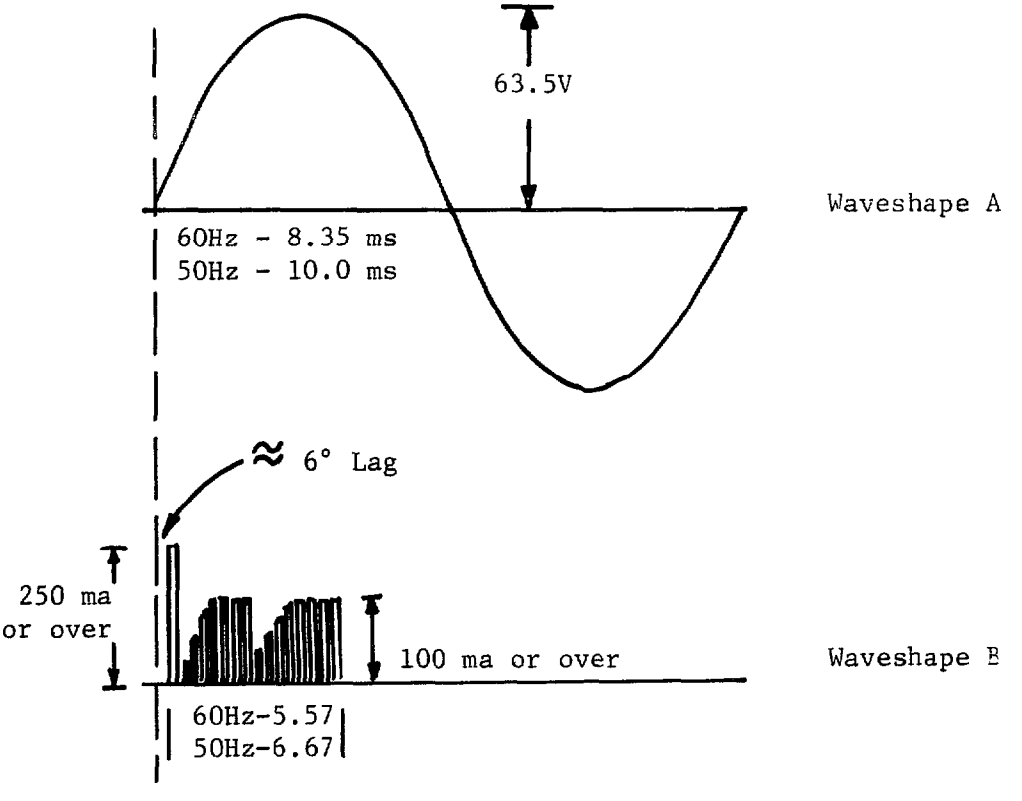
   a) Ensure that the process regulator and VIA are disconnected.

   b) Connect -25V d-c supply to BOI21 (REF 1) and pick up suicide relay.

   c) Use external trigger on the oscilloscope and connect to BOI3 (0°). Use both channels A and B and connect per following chart. If available use a current probe on Channel B.

Channel A	Channel B	Waveshape A	Waveshape B
BOI9 (120°)	PIAG (W)	63.5 ± 7V pk sinewave	Pulse train originating at 6° lag of Waveshape A.
BOI7 (240°)	P2AG (W)		
BOI3 (0°)	P3AG (W)		
BOI8 (300°)	N1AG (W)		
BOI4 (60°)	N2AG (W)		
BOI6 (180°)	N3AG (W)		

See TRACE D



TRACE D

d) Connect multimeter to BOI26 (Regulating amplifier output).

NOTE: For Type 1 voltage regulator connect suitable resistor across the regulating amplifier feedback to obtain finite control of the output.

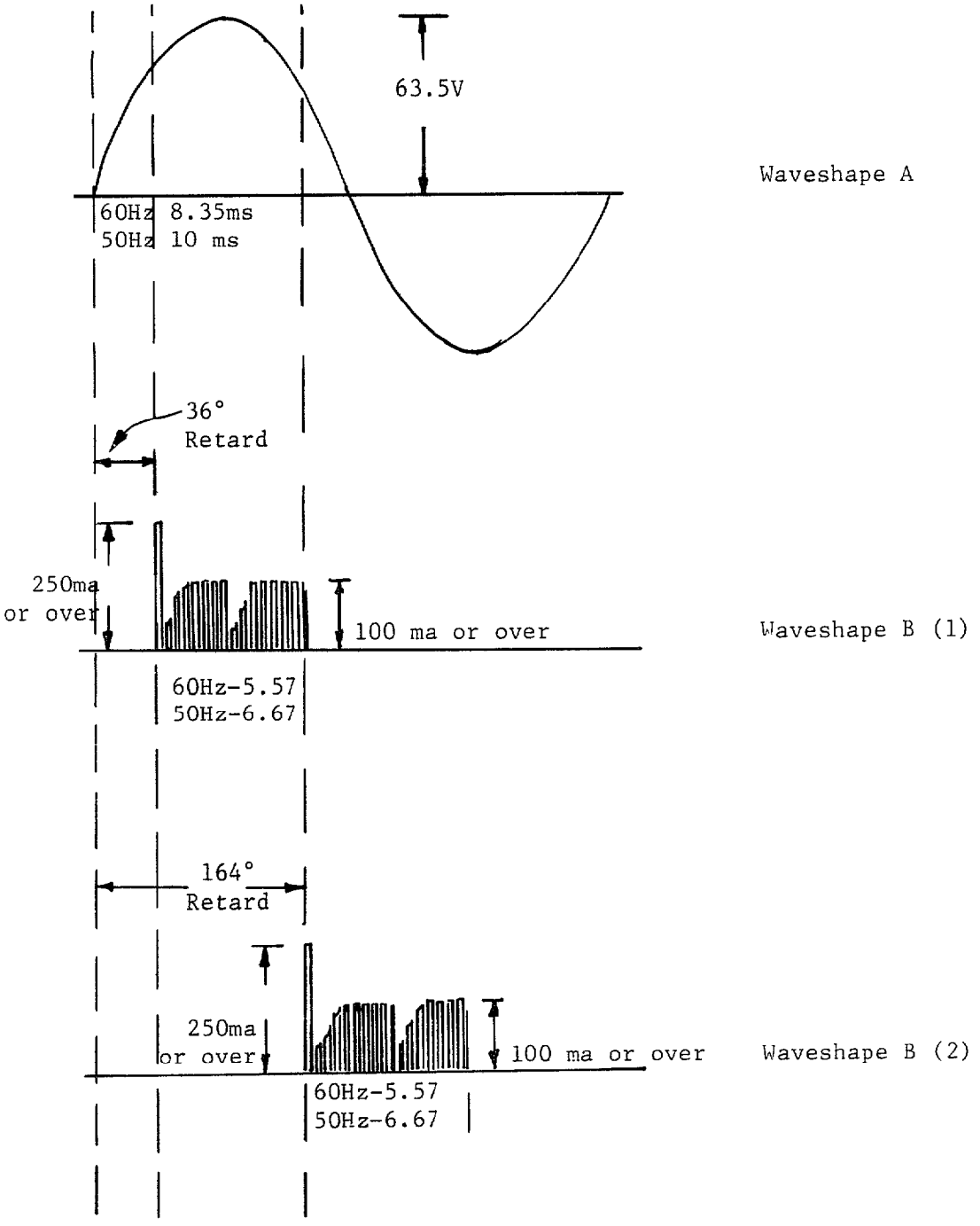
Vary the input source so that the regulating amplifier output varies from 0V to 25V DC. Observe the pulse train on Channel B and ensure that it retards smoothly in response to the input voltage change.

Check the maximum and minimum retard angle by observing the waveshapes for the following conditions:

BOI26	Chan. A	Chan. B	Waveshape A	Waveshape B
25V	BOI3 (0°)	P1AG (W)	63.5V ±7V pk. sinewave	(1) Pulse train at 36° ± 4° retard
0V	BOI3 (0°)	P1AG (W)	"	*(2) Pulse train at 164° ± 10° retard
25V	BOI9 (120°)	P2AG (W)	"	(1)
0V	BOI9 (120°)	P2AG (W)	"	(2)
25V	BOI7 (240°)	P3AG (W)	"	(1)
0V	BOI7 (240°)	P3AG (W)	"	(2)
25V	BOI6 (180°)	N1AG (W)	"	(1)
0V	BOI6 (180°)	N1AG (W)	"	(2)
25V	BOI8 (300°)	N2AG (W)	"	(1)
0V	BOI8 (300°)	N2AG (W)	"	(2)
25V	BOI4 (60°)	N3AG (W)	"	(1)
0V	BOI4 (60°)	N3AG (W)	"	(2)

See TRACE E

*The pulse train retard angles should match each other to within 2°. Absolute retard angle may vary Siltrol to Siltrol.


63.5V
Waveshape A
60Hz 8.35ms
50Hz 10 ms
36°
Retard
250ma
or over
100 ma or over
Waveshape B (1)
60Hz-5.57
50Hz-6.67
164°
Retard
250ma
or over
100 ma or over
Waveshape B (2)
60Hz-5.57
50Hz-6.67

TRACE E

8. Current Feedback Ia, Ib, I_L Suppression Bias, Lockout.

a) Connect a variable d-c source to BOI16 (Ia) and BOI50 (ACOM) and monitor it with a multimeter. Connect Channel A of the scope to BOI11 (BIAS A).

b) Slowly vary the variable supply voltage as shown below. The monitor should act as follows: If coordination card is connected for AUTO RESET

Var. Supply	BIAS A	Light DSI
0	-48V	OFF
+.3V ±.1V	- 9.75V	OFF
* IOCMa	-48V	OFF
1.2 IOCMa	-48V	ON
0	-48V	ON

Push reset PB to put light DSI off.

If coordination card is connected for Man. Reset

0	-48V	OFF
+.3V ±.1V	- 9.75V	OFF
* IOCMa	-48V	ON
0	-48V	ON

Push reset button to put light DSI off.

0	-48V	OFF
1.2 IOCM	-48V	ON
0	-48V	ON

* See system elementary for value of IOCMa.

c) Set variable supply to feedback current indicated on system elementary so that BOI20 (I_L) equals 15V. For fine adjustment adjust R16 on BOD.

9. Inverter Limit

a) Connect a variable d-c supply to REF 1 and monitor with a scope as follows:

REF 1	Chan. A	Chan. B	Waveshape A	Waveshape B
+15 volts	BOI6 (180°)	P1AG (W)	63.5V ± 7V pk sinewave	Pulse train at 5° nominal retard
"	BOI8 (300°)	P2AG (W)	"	"
"	BOI4 (60°)	P3AG (W)	"	"
"	BOI3 (0°)	N1AG (W)	"	"
"	BOI9 (120°)	N2AG (W)	"	"
"	BOI7 (240°)	N3AG (W)	"	"

b) Connect signal equal to approximately 90% IOC to BOI16 (Ia) the pulse train should advance to 4° advance ± 2°. See TRACE F. Waveshape B (1) and B (2).

10. Bridge Power Output Tests - Resistive Load - Open Voltage Loop

a) Ensure all power is off and connect the power bridge to the transformer secondary. Remove gate pulse amplifier card B1B.

b) Select magnetics etc. so that M contactor is picked up and load is connected.

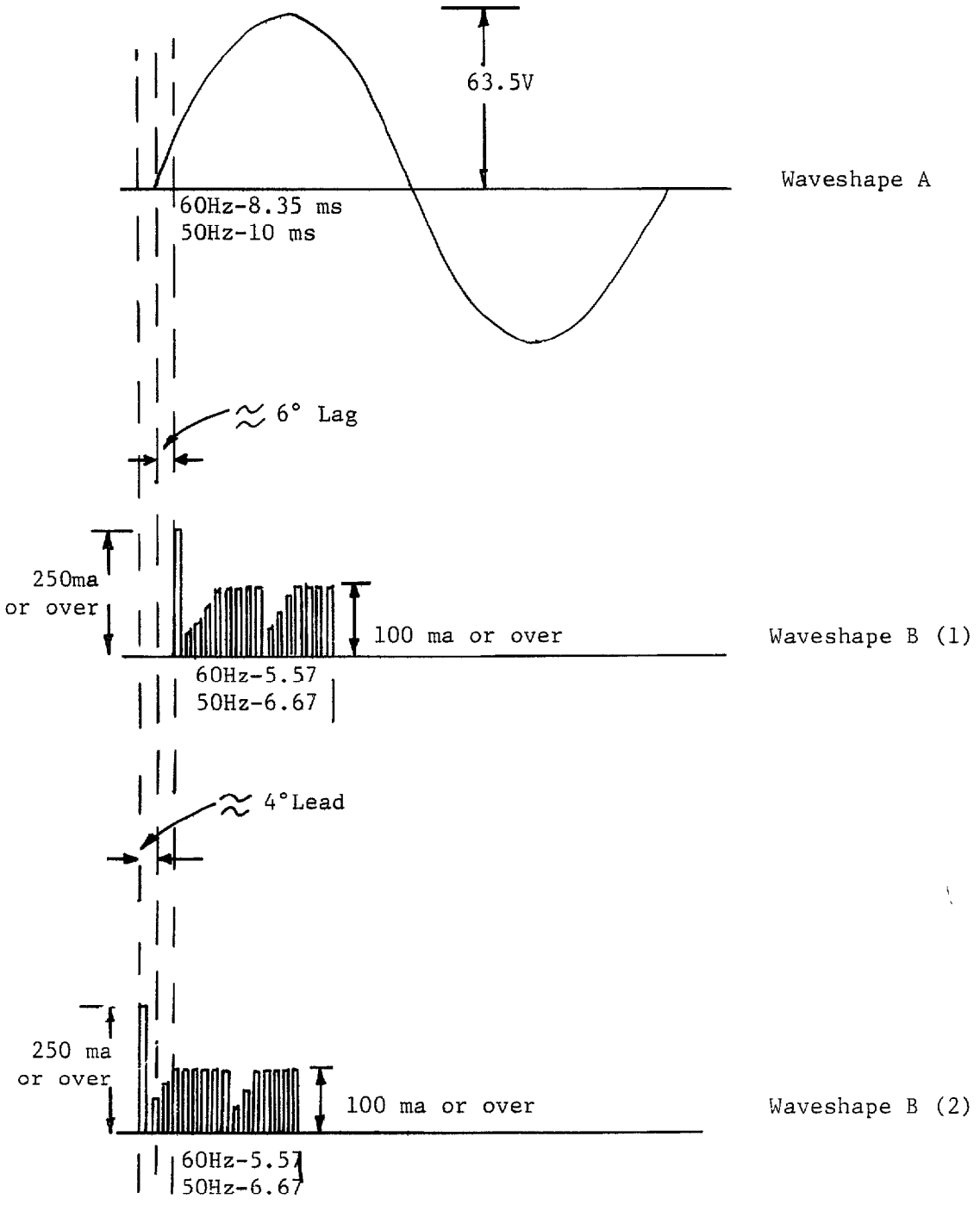
c) Reapply power and check that voltage and current meters are at zero and all neon lamps 1LP1, 2, 3 and 1LN1, 2, 3 are burning.

d) Remove power and reinsert card B1B (TPAB)

e) Connect the scope across P and N in differential mode and ground the case of the scope.

f) Reapply power and vary the reference (REF 1) so that the regulating amplifier output varies from 0 to -25V.

g) Check calibration of current feedback by comparing actual current in the load against voltage produced at BOI20 (I_L). For calibration adjust R16 on CCB, slot BOD.


63.5V
Waveshape A
60Hz-8.35 ms
50Hz-10 ms
≈ 6° Lag
250ma
or over
100 ma or over
Waveshape B (1)
60Hz-5.57
50Hz-6.67
≈ 4°Lead
250 ma
or over
100 ma or over
Waveshape B (2)
60Hz-5.57
50Hz-6.67

TRACE F

11. a) Vary input so that regulating amplifier swings from 0 to +25V. Check voltage and current varies in response to input for any irregularity.

    b) Remove power.

12. Close voltage regulator loop. (if applicable)

    a) Reconnect VIA output.

    b) Close voltage regulator by removing "open loop" coordination card (BOH) and inserting drive coordination card. (If "open loop" card was not available replace jumper removed for open loop test).

    c) Reapply power and check for zero output voltage.

    d) Increase reference to -7.5V and check output voltage is 50% of rated and that VIA output is 7.5V.

    e) Connect Channel A of the scope to BOI14 (VIA) and Channel B to BOI26 (CA). Swing the reference 0 to negative. VIA should have a sawtooth wave-shape and OA output should have smooth 360 Hz ripple (300 Hz for 50 Hz systems) approximately 5 volts peak to peak in the continuous current region.