MOD-10™ MODULAR TRANSMISSION LINE PROTECTION SYSTEM

PLS

HYBRID SCHEME

DUAL FSK CHANNELS

PHASE IDENTIFIED LOGIC

for SERIES COMPENSATED LINES

GEK-90669

These instructions do not purport to cover all details or variations in equipment nor provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with resect to local codes and ordinances because they vary greatly.

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Cover Photo: 8043805

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Introduction

MOD-10 PLS1 MODULAR TRANSMISSION LINE PROTECTION SYSTEM

PLS1 MOD-10 System for Single Pole/Three pole Tripping Applications

The PLS1 MOD-10 System is a polyphase, high speed, multi-zone directional comparison pilot relaying scheme for transmission line protection. The distance, directional, and overcurrent measuring units operate on combinations of positive, negative, and zero sequence quantities. The PLS design is based on the well proven principles used in GE's SLYP-SLCN/SLYP-SLYN MODIII static terminal equipments and adds enhancements with new design concepts and techniques.

The PLS1 provides excellent performance on series compensated lines, lines adjacent to series compensated lines, and uncompensated lines. The PLS is able to detect high resistance ground faults and is immune to the effects of zero sequence mutual coupling. The phase selectors perform reliably to provide single pole tripping with the added benefit that no user settings are required. When intercircuit faults on double circuit lines are judged likely to interfere with the phase selection process special phase-identified scheme logic can be supplied which, coupled with the necessary channel equipment, will provide reliable phase selection.

The measuring units of the PLS use an amplitude comparator coupled with an integrator - designated an "energy comparator" - which provides an operating time based on fault severity. This permits operating time in the order of 3-4 milliseconds for close-in severe faults that will be most critical to system stability.

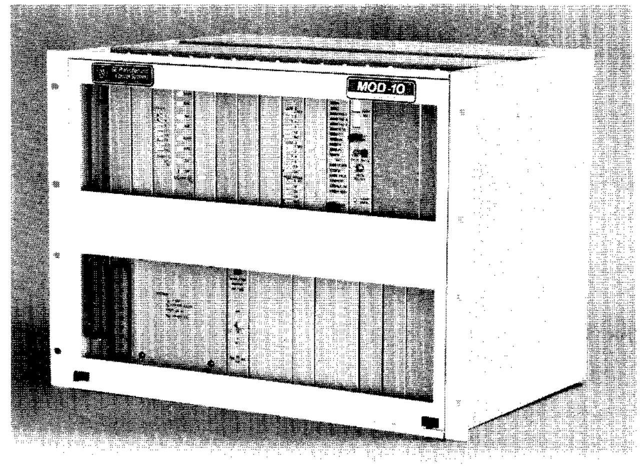
The entire PLS system is supervised by a fault detector function which prevents operation unless a system disturbance has occurred.

A Microprocessor Monitoring Interface (MMI) module is available to provide instantaneous notification of any abnormal conditions in the PLS as well as functional response data for each PLS trip operation.

OPERATING CHARACTERISTICS

Operating time
- Based on fault severity.
- Close-in severe faults - 3-4 milliseconds.
- Remote end faults - 16-24 milliseconds.

Application
- Series compensated or uncompensated lines.
- Single-pole tripping.
- High sensitivity for ground faults- can detect fault resistances up to 700 ohms for a radial feed condition.
- Suitable for two or three terminal lines.



DESIGN FEATURES

- Use of programmable logic devices (PLDs) to implement combinational logic.
- Use of "energy comparators" for measuring units.
- Line pickup (close into fault) circuit.
- Out-of-step blocking.
- Fault detector.
- Optional MMI module.

The Microprocessor Monitoring Interface (MMI) module continuously monitors up to 40 points in the PLS system. The MMI module compares the status of the fault detector with the status of the monitored points to recognize abnormal conditions in the PLS. This information is stored in non-volatile memory until accessed and/or removed by the user. The MMI module is also activated when a trip occurs and stores in a separate area of non-volatile memory all of the monitored internal responses associated with the trip. Trip data for up to five events can be stored. Trip data and monitor data are accessed by pushing a button and viewing an LCD display located on the front panel of the module. Data can also be accessed remotely via an optional RS232 interface available with the MMI.

HARDWARE & PACKAGING

Draw-out modular construction
- Plug-in modules for test and maintenance.
- Standard modular test connection plugs for current/voltage injection testing.

High-reliability components
- 168 hour burn-in of active semiconductors.
- Conservative derating for long life.

Suitable for harsh environment
- Temperature: - 20°C to + 65°C ambient.
- IEEE/ANSI SWC surge tests (C37.90.1).
- GE RFI interference test.
- IEC surge withstand test.

MOD-10™ PLS1 MODULAR TRANSMISSION LINE PROTECTION SYSTEM

TECHNICAL DATA

Ratings

Voltage	110/120 vac
Frequency	50 or 60 hz
Current	I_N = 1 or 5 amperes
DC control	48v range: 34 to 60 volts 110/125v range: 88 to 156 volts 220/250v range: 176 to 300 volts

Maximum Permissible Currents

Continuous	2 x I_N
Three second	50 x I_N
One second	100 x I_N

Insulation Test Voltage	2 kV 50/60 hertz, one minute
Impulse Voltage Withstand	5 kV peak, 1.2/50 milliseconds, 0.5 joule
Interference Test Withstand	1 MHz, 2.5 kV peak, decay time of 3 to 6 cycles to 1/2 value.
Trip Output Contacts	Continuous rating = 3 amperes Make and carry for tripping duty = 30 amperes (per ANSI C37.90) Break 180 VA resistive @ 125/250 VDC Break 60 VA inductive @ 125/250 VDC
Thyristor (SCR)	Same as trip contacts except no interrupting rating
Auxiliary Contact Ratings	Continuous rating = 3 amperes Make and carry for 30 seconds = 5 amperes Break 25 watts inductive @ 125/250 VDC Maximum: 250volts or 0.5 amperes
Ambient Temperature Range	Storage: -30 to +75 degrees C Operation: -20 to +65 degrees C
Humidity	95% without condensing
Weight	45 pounds (20 kilograms)
Dimensions	
Height	14 inches (356 millimeters) 8 rack units
Width	19.1 inches (484 millimeters standard 19 inch rack
Depth	16 inches (406 millimeters

NOMENCLATURE SELECTION GUIDE

PLS Single-Pole Tripping Models

PLS1B********B

1	Single pole tripping schemes
B	8 rack unit case
1	1 ampere rated current
5	5 ampere rated current
5	50 hz rated frequency
6	60 hz rated frequency
A	Hybrid scheme dual FSK channels phase identified channel logic
B	Hybrid scheme dual FSK channels 1P/3P channel logic
C	Hybrid scheme single FSK channel
X	Special customer logic
0	48 vdc
1	110/125 vdc
2	220/250 vdc
CL	Suitable for series compensated lines
UL	Suitable for long, uncompensated lines
UB	Suitable for short, uncompensated lines: Z1 = 0.25-6.25; Z2 = 2-50
XX	Special customer reach/application
1	Solid state tripping outputs(SCR)
2	Contact tripping outputs
A	No options
B	Continuous monitor
C	12 additional DLA points (24 total)
D	Continuous monitor and 12 additional DLA points (24 total)
X	Special customer options
B	Revision level

Sample:

PLS1B56B0UL1BB - PLS Rated 5 amps, 60 Hz, 48 vdc, suitable for single pole tripping on long, uncompensated lines, dual channel logic, (1 pole/3 pole), SCR output, MMI continuous monitor, revision B

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Scheme Description

SCHEME DESCRIPTION

This logic description applies to a PLS relaying system configured as a hybrid scheme that utilizes phase-identified communication channels to implement single-pole tripping. The scheme requires two separate frequency shift channels (power line carrier or audio tone) or one three-frequency channel to implement the phase identification.

This description applies to logic diagram 0153D7726. The logic has been simplified and reduced to the following areas as an aid in explaining the scheme performance:

1. Directional Comparison Logic
2. Weak Infeed/Repeat Keying/Line Pickup/Out-of-Step Logic
3. Trip and Reclose Logic
4. Channel Logic
5. Phase Selection Logic

Each of these areas will be described separately.

DIRECTIONAL COMPARISON LOGIC

The directional comparison logic is configured as a hybrid scheme and is used to determine whether the fault is internal or external to the protected transmission line. For internal faults, a permissive trip signal will be issued and the phase selection circuitry will then initiate tripping of the faulted phase for single-line-to-ground faults or all three phases for multi-phase faults.

Under normal conditions (infeed at all terminals of the transmission line that is sufficient to operate the tripping functions) a hybrid scheme operates exactly like a permissive overreaching transferred tripping scheme. For internal faults, one or more of the tripping functions at each terminal of the line will detect the fault and will permit keying of the appropriate transmitter or transmitters (described later) as identified by the fault type. Receipt of the phase-identified trip signal <u>and</u> operation of one or more of the tripping functions will produce a permissive trip output at each terminal of the line. Phase selection logic (described later) will then initiate tripping of the appropriate phase(s). If, for an internal fault, the infeed at one or more of the terminals is insufficient to operate at least one of the tripping functions, then a permissive tripping scheme would not operate because it is necessary for the fault to be detected at all terminals of the line. A hybrid scheme uses blocking functions along with additional logic to overcome this deficiency by allowing the trip signal received from a strong terminal to be echoed (repeated) at the weak terminals and so allow the strong terminals of the line to be tripped. The weak terminals may then be tripped by weak infeed circuitry to be described later. The signal can be repeated at the weak terminals only if the blocking functions have not operated; i.e., the signal will be repeated for internal faults only. For external faults, one or more of the blocking functions will operate to block the repeat of the signal thus tripping will be blocked at all terminals of the line.

Figure SD-5, (Sh. 1 of 0179C7549) shows the directional comparison logic for the PLS hybrid scheme. The following functions are used in the scheme:

Permissive Tripping
- PDT - positive sequence distance
- NDD - negative sequence distance
- NT & IT - negative sequence directional and overcurrent

Blocking
- PDB - positive sequence distance
- NB & IB - negative sequence directional and overcurrent

Direct Tripping
- PD1 - positive sequence distance
- ND - negative sequence distance
- IDT - zero sequence overcurrent with positive sequence restraint
- ITOC - time overcurrent backup (zero sequence with positive sequence restraint)

For an internal fault, one or more of the tripping functions will operate and apply one of the inputs to the comparer AND16 and to produce a permissive keying output via OR10, AND15, and OR18. Receipt of a trip signal at CC1 or CC2 will apply another of the inputs to the comparer while the NOT input will be absent because the blocking functions will not have operated for this internal fault. A trip permission output will then be produced via AND16, OR14, TL1, OR15, AND17 and OR16.

The channel echo (repeat) circuitry, made up of either receiver, timer TL11 and AND34 works as follows: if a trip signal is received at CC1 or CC2 and there is no output from the blocking functions the NOT inputs to AND34 will be absent. AND34 will thus produce a permissive keying output via OR18 for the 50 millisecond pickup time of timer TL11. After 50 milliseconds, no further keying will be permitted because timer TL11 will time out and apply a NOT input to AND34 to stop keying. Thus TL11 and it NOT input to AND34 perform a knockdown circuit to limit the length of time that a permissive signal will be repeated.

A priority system is used between the tripping and blocking functions to establish transient blocking during fault current reversals following clearing of an external fault on a parallel line. For an external fault, PDB or NB will operate and:

1. Apply the NOT input to AND15 to block transmitter keying.

2. Apply the NOT input to AND16 to block pilot tripping.

3. Energize timer TL30/24 or TL25 respectively.

These timers are set with a long dropout (time delay dependent on the application) so that when the fault is cleared the NOT inputs to AND11, AND15 and AND16 will not be removed immediately. Consequently, transmitter keying and pilot tripping will be prevented even if one or more of the tripping functions were to momentarily operate on a current reversal. Note that the operation of the tripping functions will cause the blocking functions to reset by applying a NOT input to AND2 and/or AND65 but that the reset will not be complete until the dropout time of the respective blocking function timer. The NOT inputs to AND2 and AND65 are required during the initial occurrence of an internal fault. For this condition the blocking functions must not produce an output else tripping would be blocked. For example, for a close-in internal three-phase fault, the blocking function (PDB) may try to operate because it is offset to include the relay location within its operating characteristic. The tripping function (PDT) will also operate however, and by virtue of its design will operate faster than the blocking function. PDT will block PDB operation by applying the NOT input to AND65 and will also block NB operation by applying one of the NOT inputs to AND2. Note that NB may try to operate on the negative sequence quantities produced during the asymmetrical occurrence of the three-phase fault, thus the reason for inhibiting it with PDT. A similar priority system is established between NT and NB and is used primarily during unbalanced faults during which PDT is unlikely to operate. PDT will also initiate fast reset of timer TL30/24 in the event that NB operated before PDT on the occurrence of an internal three-phase fault.

The PDX function (not shown on the simplified logic diagram) has a separate reach adjustment from the other positive sequence distance functions and is used with a separate timer to provide an independent zone 2 function that can be set to coordinate with zone 1 functions in adjacent lines.

The direct tripping functions listed previously operate to trip directly and independently of the pilot portion of the scheme. The output of any of these functions will initiate trip permission directly through OR214, OR14, OR15 and AND17.

WEAK INFEED/REPEAT KEYING/LINE PICKUP TRIP/OUT-OF-STEP LOGIC

Simplified logic for the weak infeed trip circuitry is shown in Fig. SD-6, (Sh. 2 of 0179C7549) and is composed of AND14, any receiver (via OR12), OR11, OR37 and TL16. Assume that an internal fault has been detected at the remote terminal of a transmission line and that the local blocking functions have not operated. Therefore, the receiver at the local terminal will be producing an output and there will be no output from OR37 because none of the blocking functions are up. If the fault detector (FD), or the overcurrent blocking supervision function (IB), or the overcurrent tripping supervision function (IT) are picked up, or if all three voltage detectors are dropped out, then OR11 will produce an output. Consequently, AND14 will have all of its upper inputs present, and if it is assumed for the moment that the lower input to AND14 is present, then AND14 will produce an output. This output is applied to security timer TL16 which will issue a trip permission when it times out.

The lower input to AND14 comes from the open-pole sequencing circuitry which is required to allow the weak infeed circuitry to perform at the inception of a fault, to remove it from service during the open-pole period and to re-insert it on the inception of a fault during or following the open-pole period. The circuitry works as follows. At the inception of a fault, NOT4 will be producing an output thus the lower input to AND14 will be present, and tripping will be as described above. When the faulted phase is tripped, timer TL26 will time out to apply the middle input to AND214 via OR211 and to inhibit any phase selector output which in turn applies the upper input to AND214 via NOT212 and OR212. When the faulted phase is cleared by opening the breaker, the respective open-pole detector (AND7, AND8, or AND9) will pick up and apply the lower input to AND214 via OR32. AND214 will thus produce an output which will be sealed in on the open-pole detector via OR211 and OR212. The output of AND214 without a concurrent phase selector output will allow AND71 to produce an output which will reset NOT4 and thus remove the lower input from AND14 so that weak infeed tripping will be blocked. If a subsequent fault occurs during the open pole period, one of the phase selectors will pick up and apply the NOT input to AND71 via OR210. NOT4 will then produce an output which will apply the lower input to AND214 thus re-instating weak infeed tripping. If no fault occurs, weak infeed tripping will be re-instated when the open-pole detector resets after the breaker is successfully reclosed.

Timer TL27 (following AND214) will be energized during the open-pole period and its output is used to arm the three-pole tripping circuitry so that any faults occurring during the open-pole period, or during reclosure of the breaker will be tripped three-pole

The line pickup logic is used to initiate tripping when a line is energized by a manual closure or on reclosing following a three-pole trip. The circuitry is composed of AND41, TL4, TL7, AND42, TL8, OR42, OR41, AND60, AND43 and CC6. The circuitry works as follows. AND41 will produce an output when the line is de-energized as indicated by outputs from <u>all three</u> open-pole detectors. At that time, timer TL7 will be energized and when it times out 150 milliseconds later, it will apply the top input to AND42 and the bottom input to AND60. The line pickup circuit is now armed and ready to trip if any of the following functions pick up when the line is energized:

1. PDT - positive sequence tripping function
2. NDD - negative sequence tripping
3. I1T - positive sequence overcurrent function

If none of these functions operate when the line is returned to service then timer TL7 will be fast reset 3 cycles (TL4 pickup time) after all three phase voltages return to normal as indicated by no output from OR7.

Note that neither NDD or PDT will pick up when closing into a bolted three-phase fault (such as when the grounding chains are left on the line), hence the reason for the I1T function. This function must be set to detect the minimum three-phase fault for a fault at the relay location. It is desirable to set this function above the maximum load current, however, it must be set below the maximum load current if conditions require it. Timer TL8 is provided for use in those applications where I1T must be set below full load current and where high speed reclosing is used at each terminal of the transmission line. This timer allows time for the voltage to return to normal and remove line pickup tripping from service before load current can initiate a trip following a simultaneous high speed reclose. If simultaneous reclosing is not used at each end of the line, then faster tripping can be attained on closing into a fault by applying a continuous input to CC6 which allows timer TL8 to be continuously bypassed via AND43. Timer TL8 should be bypassed if I1T can be set above full load regardless of whether or not simultaneous high speed reclosing is used.

Out-of step blocking circuitry is provided and the output is routed through 2 switches (OSB-1 and OSB-2). The output of these switches is routed through various points in the logic to prevent certain outputs during an out-of-step condition. See the overall logic diagram 0153D7740 for how these switches may be used.

TRIP AND RECLOSE LOGIC

The trip logic is used to trip the appropriate pole of the breaker following a permissive trip and associated phase selection. The simplified trip logic is shown in Figure SD-7, (Sh. 3 of 0179C7549). The logic works as follows. Trip permission from the directional comparison logic is applied to AND21A, AND21B and AND21C via OR16. For single-line-to-ground (SLG) faults, the faulted phase will only be selected. An output from the phase selection logic will apply the second input to its associated AND circuit (21A, B or C) and initiate tripping through its associated logic chain. For example, if phase "A" is faulted, then phase "A" will be selected and an input will be applied to AND21A via OR22A. The output of AND21A will initiate tripping via OR24 and AND30. Note that the second input to AND30 comes from the fault detector (FDP) that is an integral part of the PLS scheme. This fault detector will operate only for faults on or in the vicinity of the protected line and provides security by insuring that tripping cannot be initiated unless a fault has occurred within the vicinity of the protective relaying scheme. For multi-phase faults, the phase selector circuitry will issue a three-pole trip output via OR20A which will be applied to AND21A, AND21B and AND21C concurrently. If trip permission is given via OR16, then all three poles of the breaker will be tripped simultaneously.

The system logic will produce an inhibit reclose output if a trip is initiated and there is an output from any or all of the following functions which may be independently selected via an appropriate link provided in the system:

1. PDX, positive sequence distance function, zone trip
2. PDT, positive sequence distance function, pilot trip
3. PD1, positive sequence distance function, zone 1 trip
4. ND, negative sequence distance function, direct trip
5. Any multi-phase fault as indicated by the two-out-of-three selection logic
6. A direct transferred trip input from external equipment (if used, not selectable by link)

The inhibit reclose outputs are sealed in via a loss of voltage (any U/V) and are provided for use in sequential reclosing schemes; i.e., reclosing would be inhibited via this output until the voltage returns to normal at which time reclosing would then be permitted. The basic premise behind sequential reclosing is to allow the end where the fault is the least severe to reclose first and then allow the other end to follow if the reclosure is successful as indicated by the return of voltage.

The PLS System does not identify a three-phase fault only, but the following can be ascertained. The PDX and PDT functions will operate for all three-phase faults on the line and may operate for some severe unbalanced faults, including single-line-to-ground (SLG) faults if they are severe enough. Of the two functions, the PDT is the least likely to operate for SLG faults. The PD1 function will operate for all three-phase faults within its reach, for some severe line-to-line (L-L) and line-to-line-to-ground (L-L-G) faults but it will not operate for any SLG faults.

Although these outputs are designated inhibit reclose and are normally used in sequential reclosing schemes, they can alternatively be used to block reclosing. Therefore, if it is desired to block reclosing for all three-phase faults and if it is acceptable to block reclosing for some severe L-L and L-L-G faults then these contacts can be used. Note that blocking of reclosing for the severe L-L and L-L-G faults would be beneficial to the power system.

The system logic will produce a lockout reclose output if a trip is initiated and there is an output from any or all of the following selectable functions:

1. Zone 2 timer, time-delayed trip
2. Zone 3 timer, time-delayed trip
3. ITOC, time overcurrent trip
4. CC8 (external three-pole trip)

These outputs are not sealed by an undervoltage condition as are the inhibit reclose outputs, and persist only as long as a trip output is produced. They can be used to lockout reclosing by energizing the appropriate input in the reclosing relay.

CHANNEL LOGIC

Phase-identified channels are used to increase the reliability of single-pole tripping for the following conditions:

1. Series compensated lines
2. Double-circuit lines (intercircuit faults)
3. Weak infeed conditions
4. High resistance faults.

Reliability is enhanced by requiring the comparison of the local phase selection against the remote phase selection. For example, if the local phase A selector operates, then phase A tripping will be initiated if the received signal indicates that the remote phase A selector has also operated except for the case of a heavy close-in fault or a weak infeed condition as described below.

For single-pole tripping, the channels are assigned as follows:

Single-pole Tripping

	Channel	
Phase	No.1	No.2
A	x	
B		x
C	x	x

The following assignments are made to aid in three-pole tripping:

Three-pole Tripping

	Channel	
Phases	No.1	No.2
AB	X	X
BC	X	
CA		X
ABC	X	X

The channel keying circuitry is shown in Figure SD-8, (Sh. 4 of 0179C7549) and works as follows:

a. AND18 and AND19 are supervised by an output of OR18 which produces an output whenever one of the permissive trip functions operate, or when any channel signal is received and the blocking functions have not operated (a weak infeed condition exists).

b. OR352 output keys the φA (BC) channel

c. OR353 output keys the φb (CA) channel

d. OR368 output keys the φC (AB) channel

e. AND357A, B and C permit the φA, φB or φC received signals to be repeated respectively for low-level single-line-to-ground faults as indicated by an output from OR219.

f. The NOR69 input to AND357A, B and C is basically controlled by Timer TL26 which is set to time out just before the breaker opens. Keying permission is removed at that time to prevent the sending of erroneous channel signals that might result from the breaker opening.

The channel receiver circuitry is also shown in Figure SD-9, (Sh. 5 of 0179C7549). Note that the "P" and "U" outputs shown on the diagram refer to the permissive and unblock outputs respectively. This logic should be included in the receiver when the power line is used as the transmission medium. The "U" output is required to produce a receiver output in the event signal attenuation occurs as a result of a fault on the transmission line.

TRIP SELECTION LOGIC

Single-pole trip selection logic for Phase A tripping is shown in Figure SD-10, (Sh. 6 of 0179C7549). The logic works as follows.

AND314A will produce an output to trip Phase A for the following conditions:

Whenever a direct trip function operates and there is an output from the φA selector but not from the φB and φC selectors (AND373A output). Tripping is permitted under these conditions without the need for a received signal from the remote terminal because phase selection will be very reliable for faults within reach of the direct tripping functions (even for intercircuit faults).

Whenever OR16 produces an output (trip permission) and there is not a "P" output from any of the receivers. This condition will arise when the power line is used for communications and signal attenuation occurs due to a fault on the transmission line. At that time, there will be a "U" output from the receiver to activate OR16 but there will be no "P" output to activate any of the other trip selection circuits to be described next.

AND317A will produce an output to trip Phase A for the following conditions:

Whenever there is an output from the φA selector and an output from the φA receiver. This would be the normal mode of tripping in the absence of a direct trip output.

AND318A will produce an output to trip Phase A for the following conditions:

> Whenever there is a ϕA receiver output, a drop in the phase A voltage (the not VA input) and a weak infeed condition as indicated by an output from TL16. This mode of operation is provided for weak infeed conditions and a concurrent drop in voltage on the faulted phase.

AND319A will produce an output to trip Phase A for the following conditions:

> Whenever there is a ϕA receiver output, a weak infeed condition and no output from any phase selector. This mode of operation is provided for the case of very weak infeed conditions.

AND320A will produce an output to trip Phase A for the following conditions:

> Whenever there is no phase selector output and no receiver output but there is a drop in voltage and a weak infeed condition as indicated by an output from timer TL16. This mode of operation is provided if power line carrier is used and the signal is lost due to attenuation by a fault on the line.

The above situations apply to single-pole tripping with respect to Phase A. Identical circuitry is provided for phases B and C.

Three-pole trip selection logic is included in the scheme and it is shown in Fig. SD-11, (Sh. 7 of 0179C7549).

In the part of the logic shown for an AB fault, three-pole tripping will be selected if there is an output from the ϕC receiver and an output from the ϕA and ϕB selectors and no output from the ϕC selector. Similarly, three-pole tripping will be selected if there is an output from the ϕC receiver along with a concurrent drop in the ϕA and ϕB voltages without a concurrent drop in the ϕC voltage. Identical logic is provided for BC and CA faults.

Three-pole tripping will be selected by an output of PDT if the local IB function does not operate (indicating a three-phase fault) and if a three-pole trip signal is being received from the remote terminal (indicating a multi-phase fault there).

An output from NDD will also select a three-pole trip provided:

1. That the 3I0 function has not operated and there is no output from TL15 (any phase selector) as indicated by an output from AND221, or,

2. The IT function has not operated to apply the NOT input to AND203 via OR200.

This mode of operation is intended primarily for some phase-to-phase and phase-to-phase-to-ground faults in which one phase selector may have been slow in operation or may not have operated at all.

MOD 10 MNEMONIC LEGEND

BFI	BREAKER FAILURE INITIATE
BLK ZN	BLOCKING ZONE
CC	CONTACT CONVERTER
CFA	CHANNEL FAILURE ALARM
CHTR	CHANNEL TRIP
CK, CLK	CLOCK
CM	CONTINUOUS MONITOR POINT
DLA	DATA LOGGING ALARMS
FD	FAULT DETECTOR
FDP	FAULT DETECTOR SUPERVISION
FF	FUSE FAILURE
$I_{ØØ}$	PHASE TO PHASE CURRENT (MT OVERCURRENT SUPERVISION)
I_1	LINE PICKUP SUPERVISION
I_{1S}	POSITIVE-SEQUENCE SUPERVISION
I_{1T}	POSITIVE -SEQUENCE TRIPPING SUPERVISION
I_B	BLOCKING OVERCURRENT SUPERVISION
IDT	DIRECT TRIP OVERCURRENT
IM	OVERCURRENT SUPERVISION
IMA	PHASE A SENSITIVE OVERCURRENT FUNCTION
IMB	PHASE B SENSITIVE OVERCURRENT FUNCTION
IMC	PHASE C SENSITIVE OVERCURRENT FUNCTION
I_0	ZERO-SEQUENCE OVERCURRENT SUPERVISION
I_0-KI_1	ZERO-SEQUENCE OVERCURRENT WITH POS. - SEQUENCE RESTRAINT
IPB	PILOT BLOCKING
IPT	PILOT TRIPPING
IR	RECLOSE INHIBIT
IT	TRIPPING OVERCURRENT SUPERVISION
ITOC	TIME OVERCURRENT SUPERVISION
LR	LOCKOUT RECLOSE
M1	PHASE-PHASE ZONE 1 DISTANCE FUNCTION
MB	MHO BLOCKING FUNCTION
MG1	PHASE-GND ZONE 1 DISTANCE FUNCTION
MOB	MHO OUT OF STEP BLOCK FUNCTION
MT	PHASE-PHASE OVERREACHING PERMISSIVE TRIP FUNCTION
MTG	PHASE-GND OVERREACHING PERMISSIVE TRIP FUNCTION
NB	NEGATIVE-SEQUENCE BLOCKING DIRECTIONAL FUNCTION
ND	NEGATIVE-SEQUENCE DISTANCE FUNCTION
NDD	PERMISSIVE NEGATIVE-SEQUENCE DISTANCE FUNCTION
NT	NEGATIVE-SEQUENCE TRIPPING DIRECTIONAL FUNCTION
OS	OUT OF STEP
OSB	OUT OF STEP BLOCKING
PD1	POSITIVE-SEQUENCE ZONE 1 DISTANCE FUNCTION
PDB	POSITIVE-SEQUENCE BLOCKING DISTANCE FUNCTION
PDT	POSITIVE-SEQUENCE OVERREACHING DISTANCE FUNCTION
PDX	AUXILLARY ZONE POSITIVE-SEQUENCE DISTANCE FUNCTION
POSB	POSITIVE-SEQUENCE OUT-OF-STEP BLOCKING FUNCTION
PTFF	POTENTIAL FUSE FAILURE FUNCTION
RB	RECLOSE BLOCK
RCVR	CHANNEL RECEIVER
RI	RECLOSE INITIATE
SUP	SUPERVISION
TAR	TARGET
TH	THRESHOLD
TOC	TIME OVERCURRENT BACKUP
TP	TEST POINT
TR BUS	TRIP BUS
TT	TRANSFER TRIP
V_1	POSITIVE-SEQUENCE UNDER VOLTAGE FUNCTION
V_A	PHASE A UNDER VOLTAGE FUNCTION
V_B	PHASE B UNDER VOLTAGE FUNCTION
V_C	PHASE C UNDER VOLTAGE FUNCTION
V_P	POLARIZING VOLTAGE
WI	WEAK-INFEED TRIP
XMTR	CHANNEL TRANSMITTER

Figure SD-1 (0286A2774 [4]) MOD 10™ Mnemonic Legend

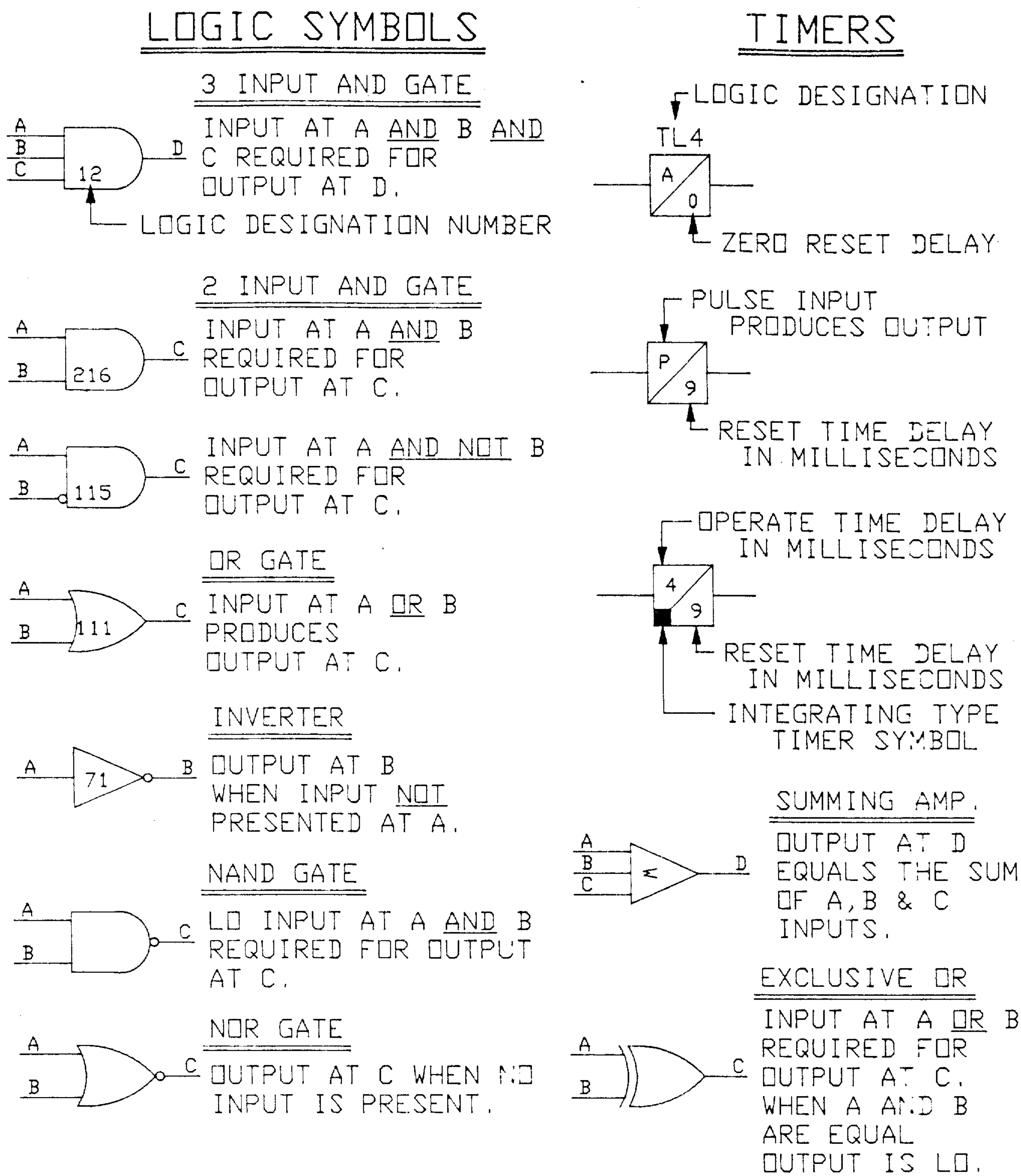
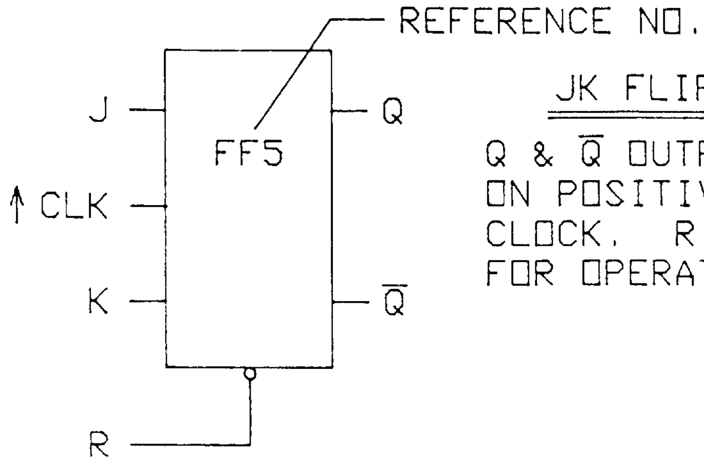


Figure SD-2 (0286A2775 Sh.1 [3]) Logic and Internal Diagram Legend

FLIP FLOPS

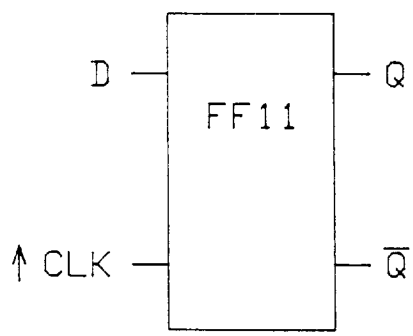


JK FLIP FLOP

Q & $\overline{Q}$ OUTPUTS OCCUR ON POSITIVE EDGE OF CLOCK. R MUST BE LOW FOR OPERATION.

TRUTH TABLE

J	K	Q
L	L	NC
L	H	H
H	L	L
H	H	TOGGLE

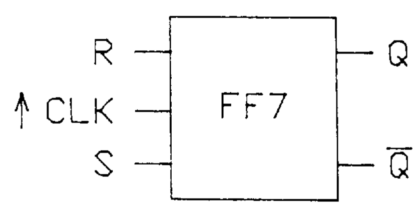


D FLIP FLOP

Q & $\overline{Q}$ OUTPUTS OCCUR ON POSITIVE EDGE OF CLOCK.

TRUTH TABLE

D	Q
L	L
H	H



RS FLIP FLOP

Q & $\overline{Q}$ OUTPUTS OCCUR ON POSITIVE EDGE OF CLOCK.

TRUTH TABLE

R	S	Q
L	L	NC
H	L	L
L	H	H
H	H	?

NOTE:
H=1 (HIGH INPUT)
L=0 (LOW INPUT)
NC= NO CHANGE
$\overline{Q}$=INVERSE OF Q

Figure SD-2 (0286A2775 Sh.2 [3]) Logic and Internal Diagram Legend

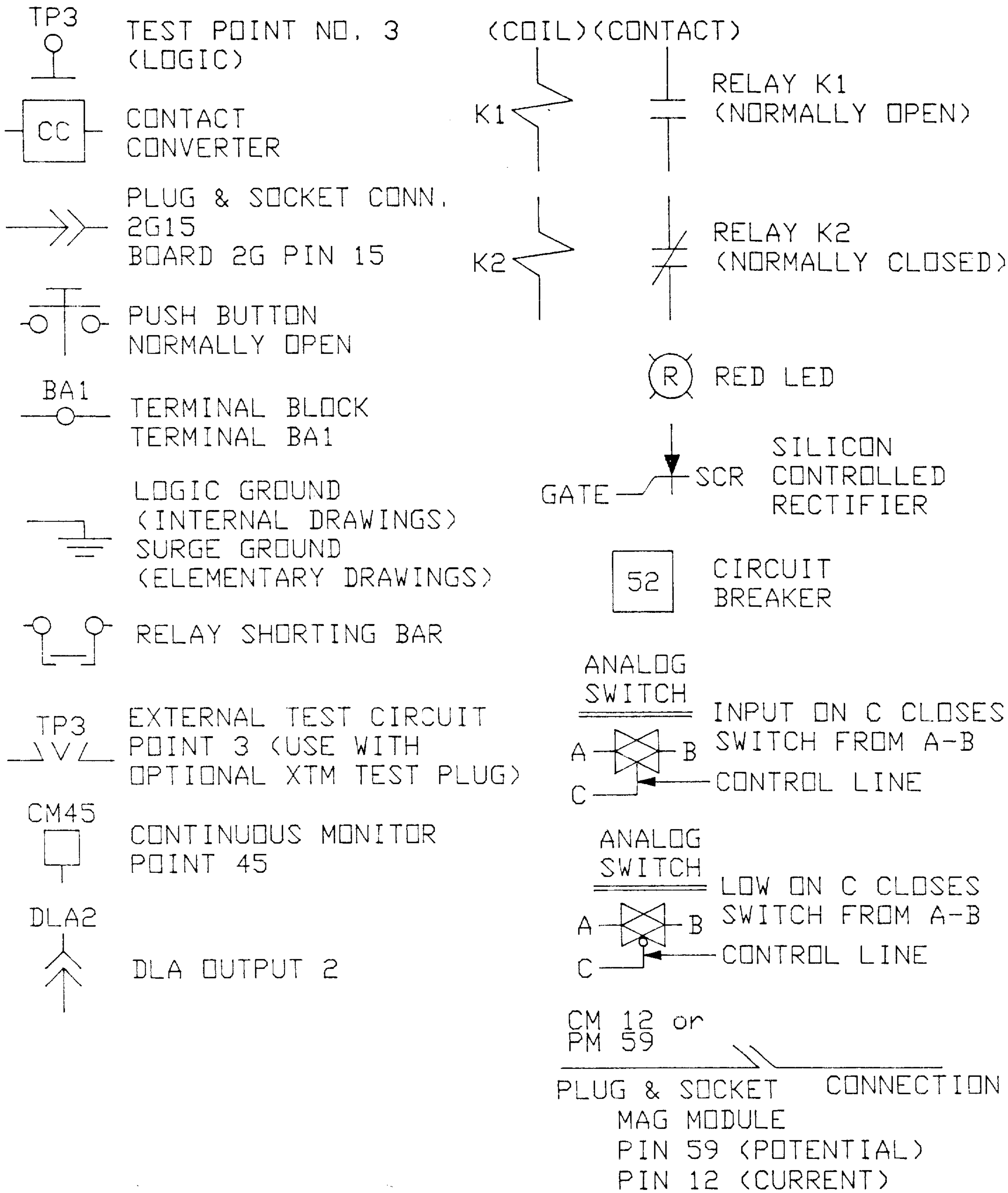


Figure SD-2 (0286A2775 Sh.3 [3]) Logic and Internal Diagram Legend

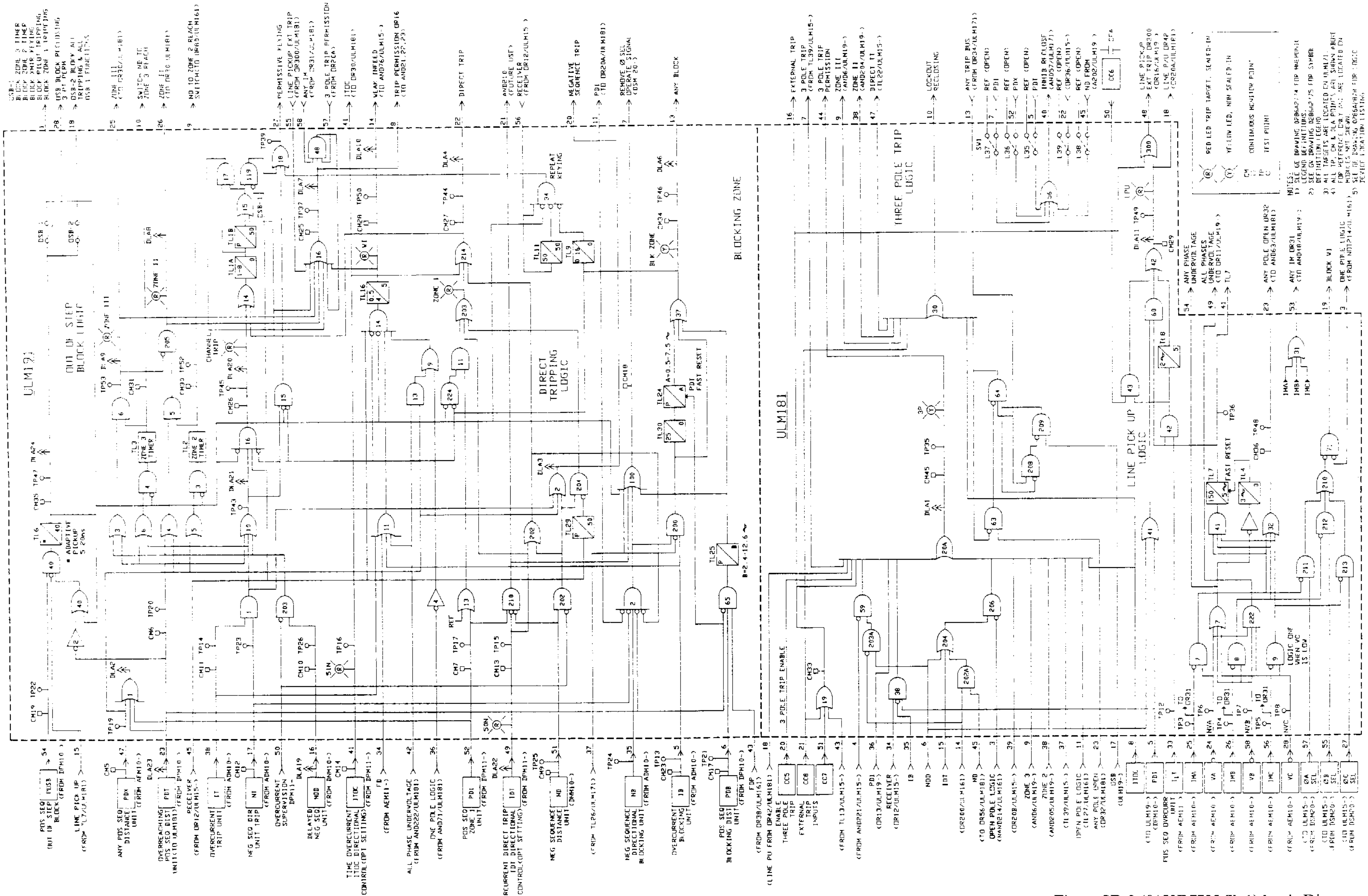


Figure SD-3 (0153D7725 Sh.1) Logic Diagram

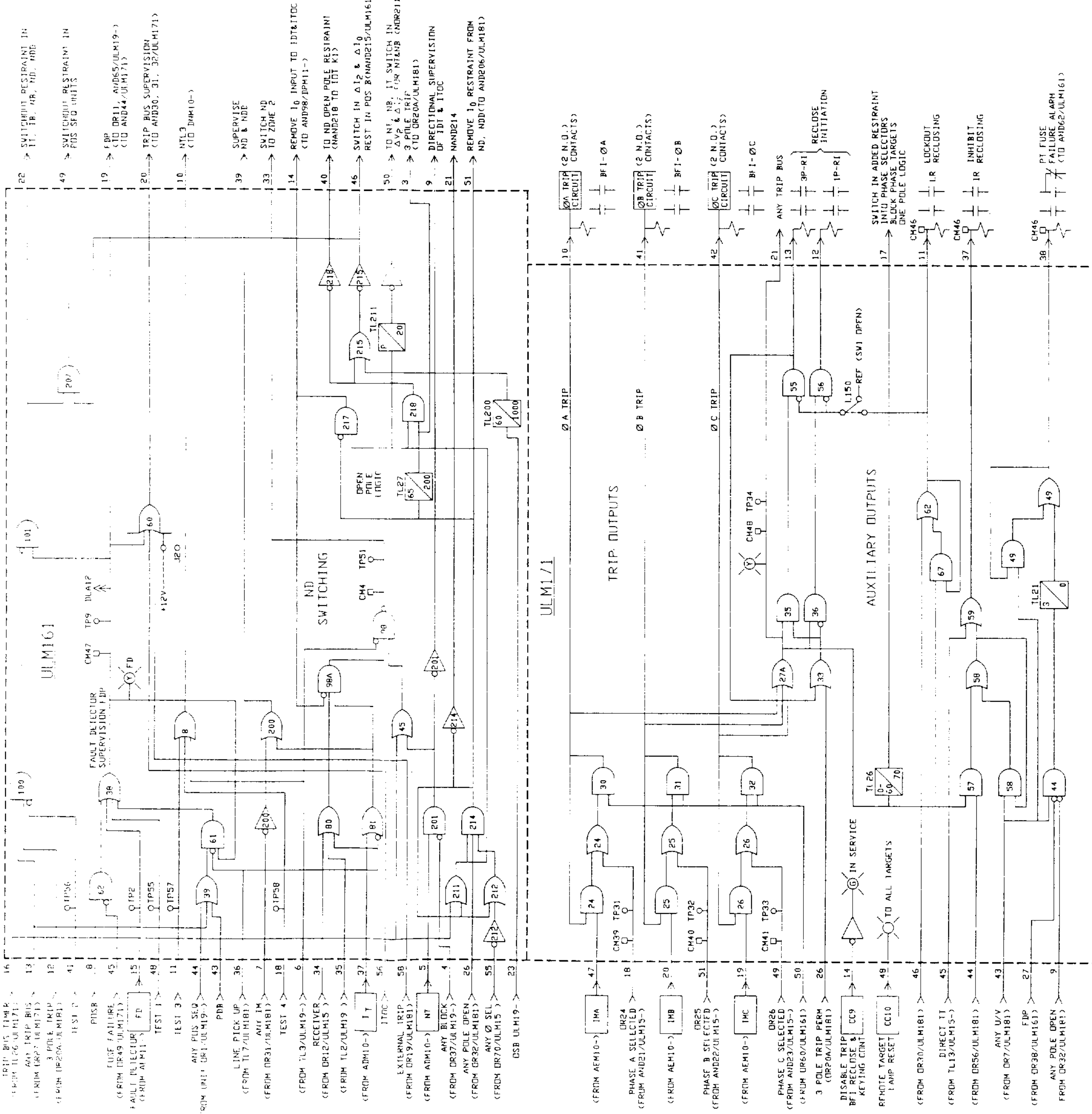


Figure SD-3 (0153D7725 Sh.2) Logic Diagram

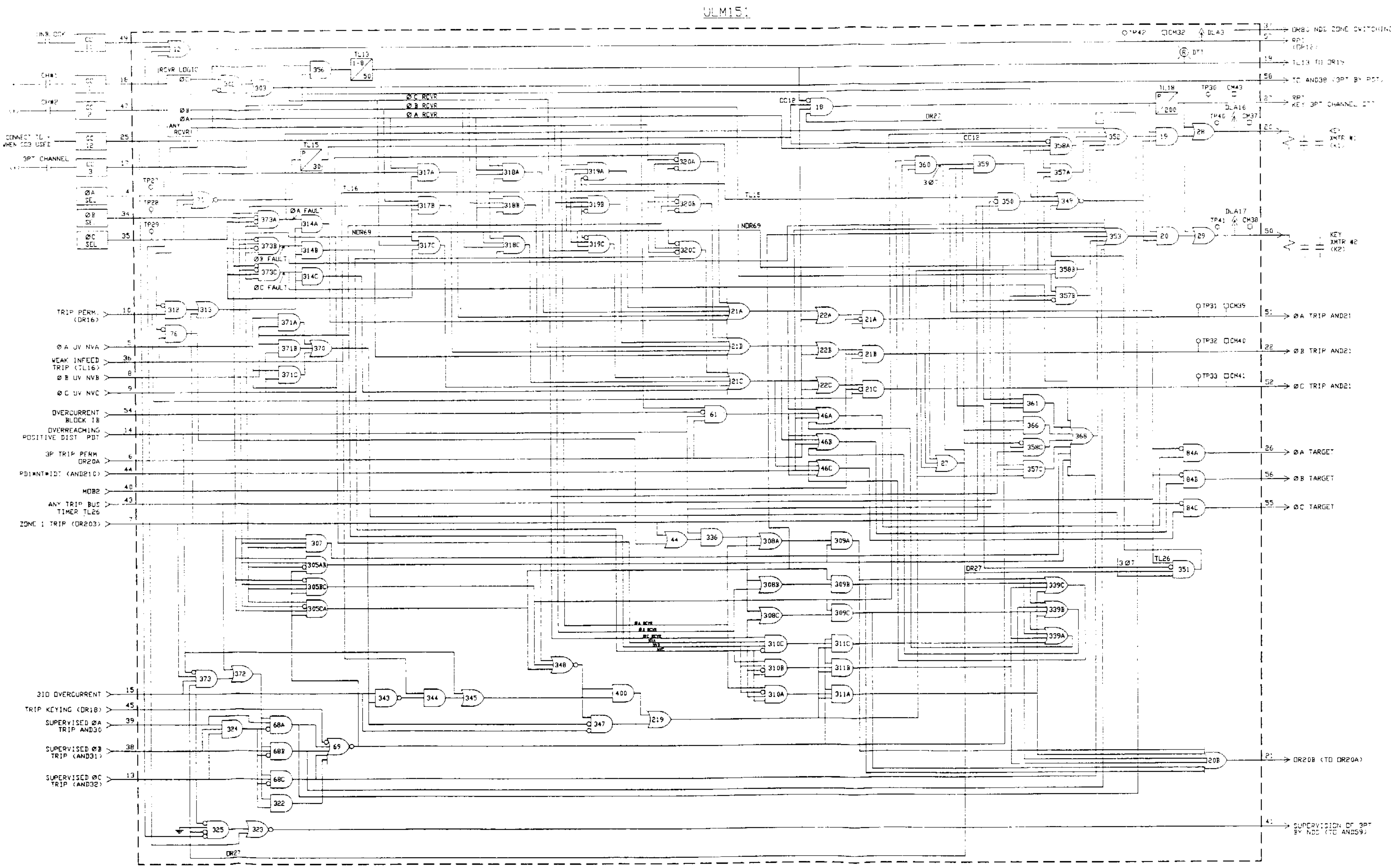


Figure SD-3 (0153D7725 Sh.3) Logic Diagram

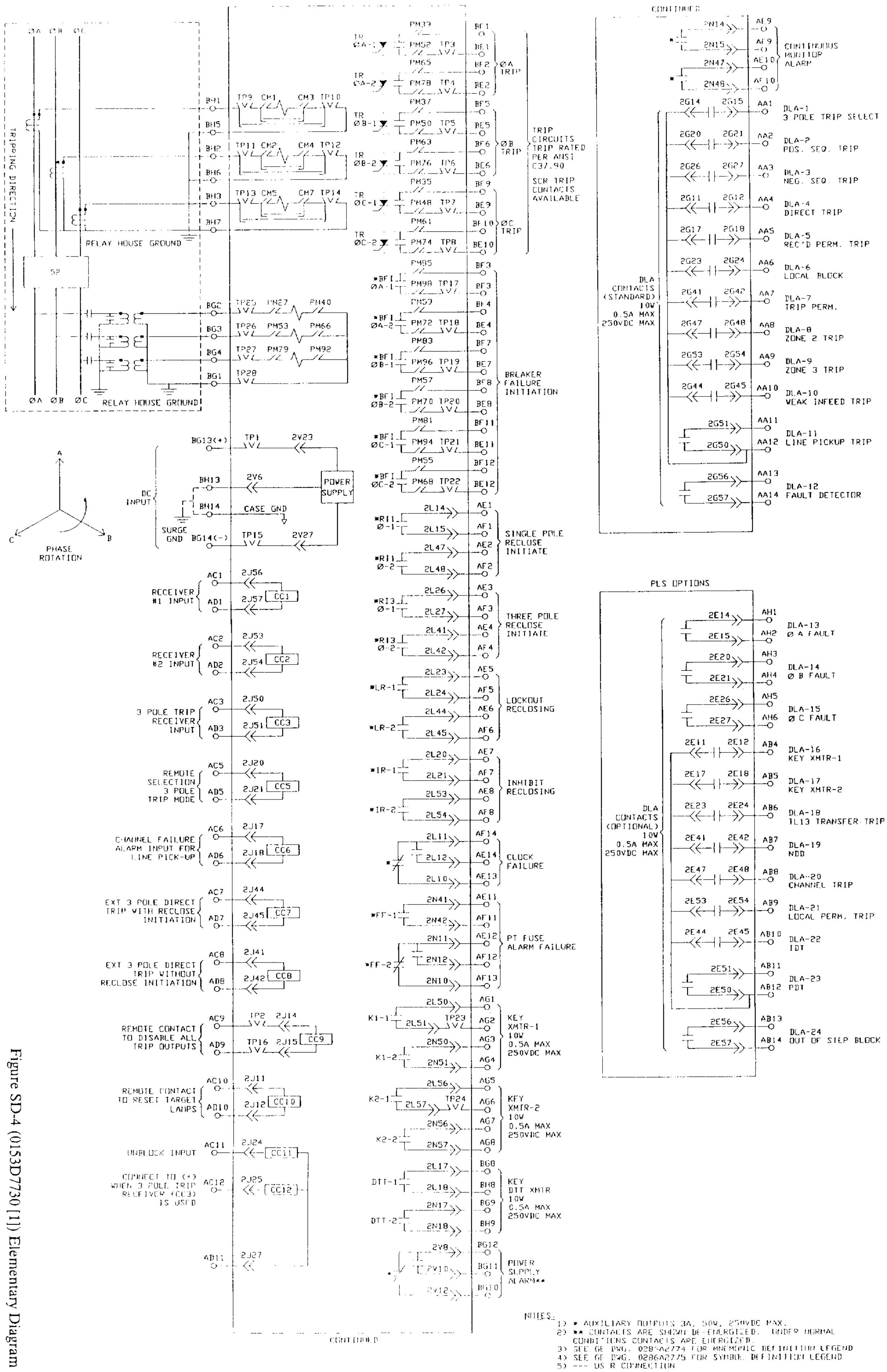


Figure SD-4 (0153D7730 [1]) Elementary Diagram

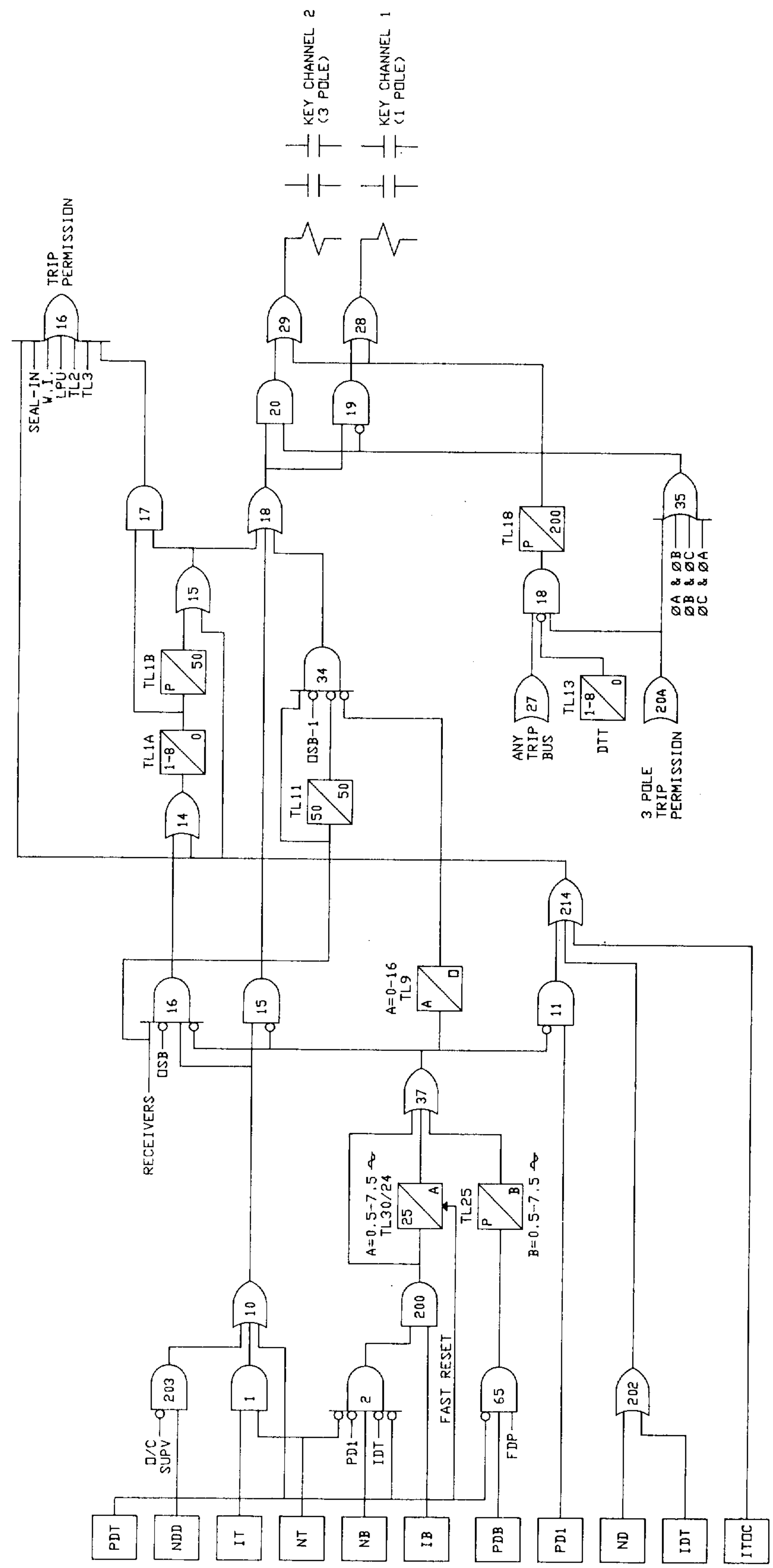


Figure SD-5 (0179C7549 Sh.1) Directional Comparison and Direct Trip Logic

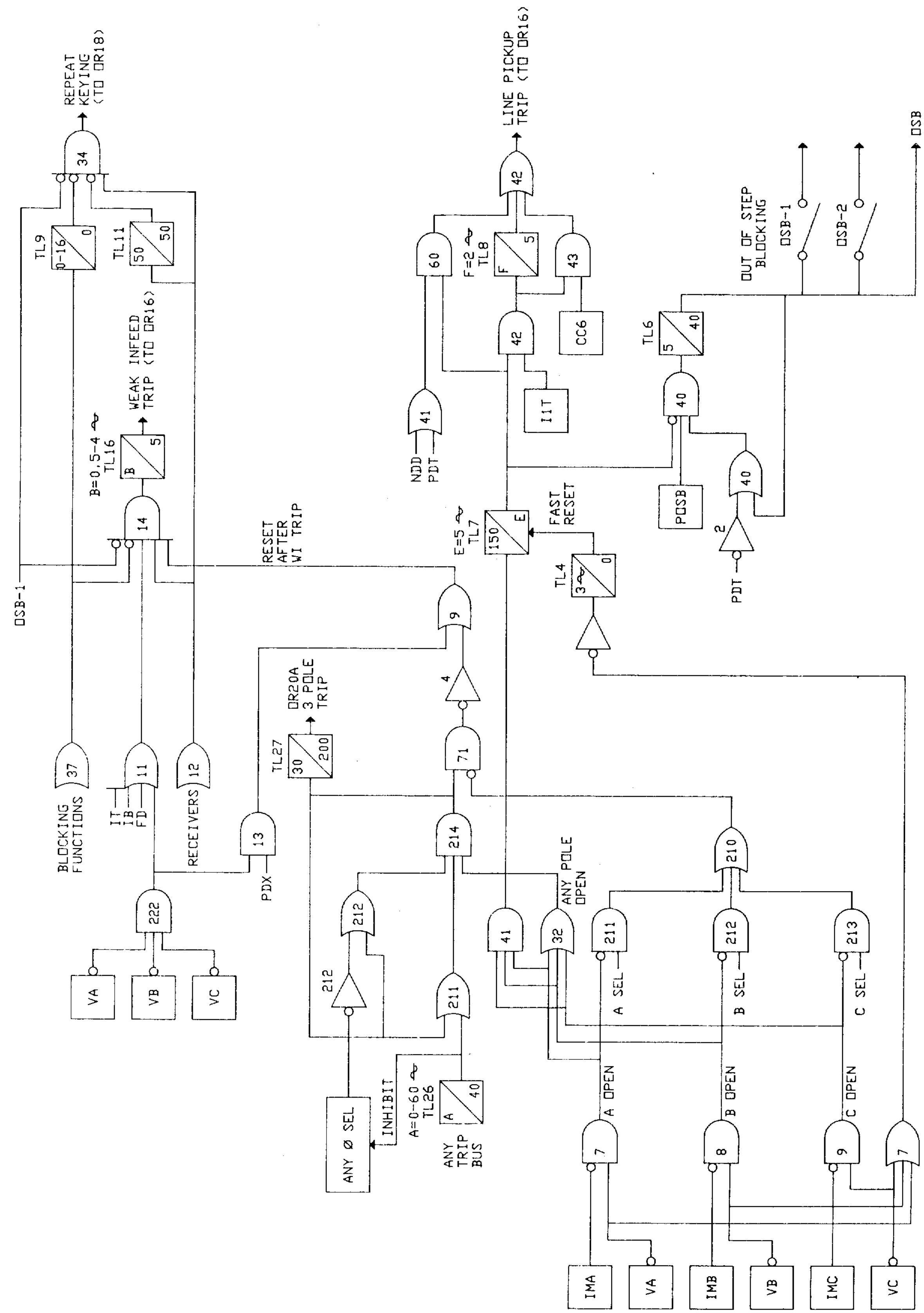


Figure SD-6 (0179C7549 Sh.2) Trip and Reclose Logic

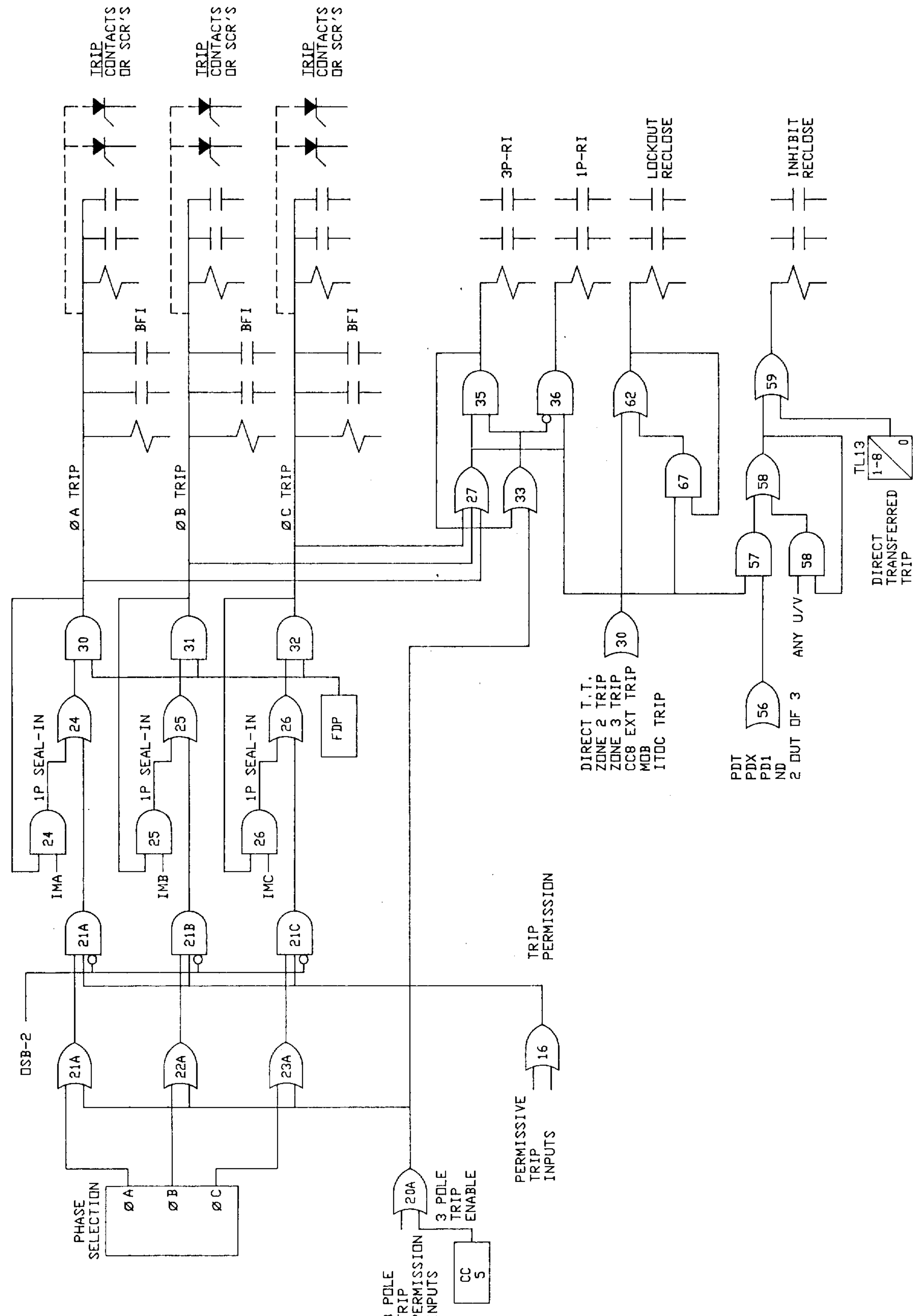


Figure SD-7 (0179C7549 Sh.3)
Weak Infeed/Repeat Key/Line PU/Out of Step Logic

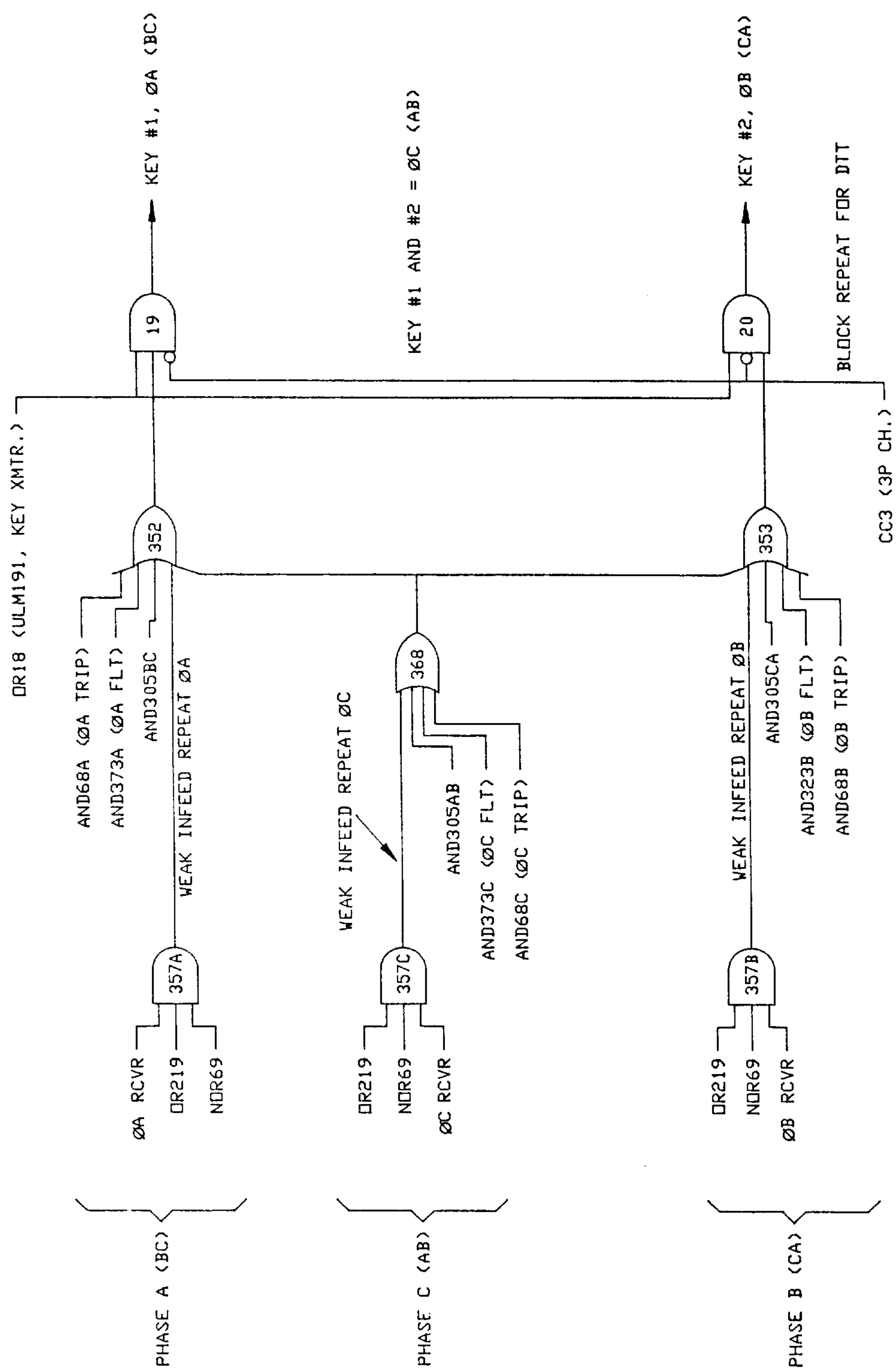
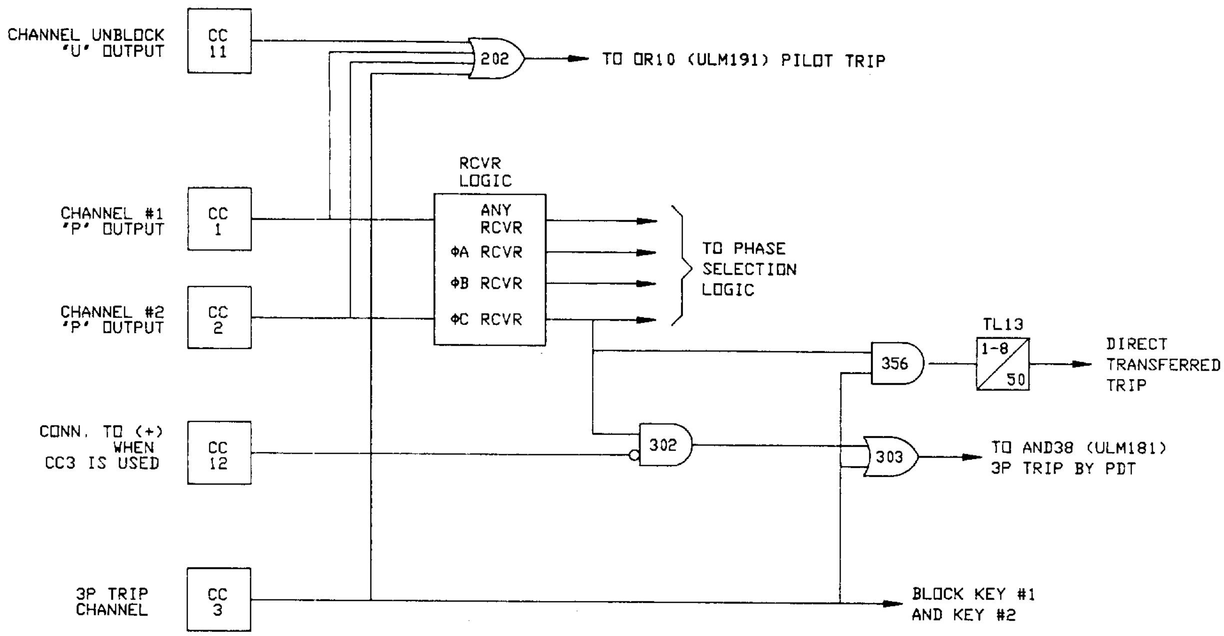
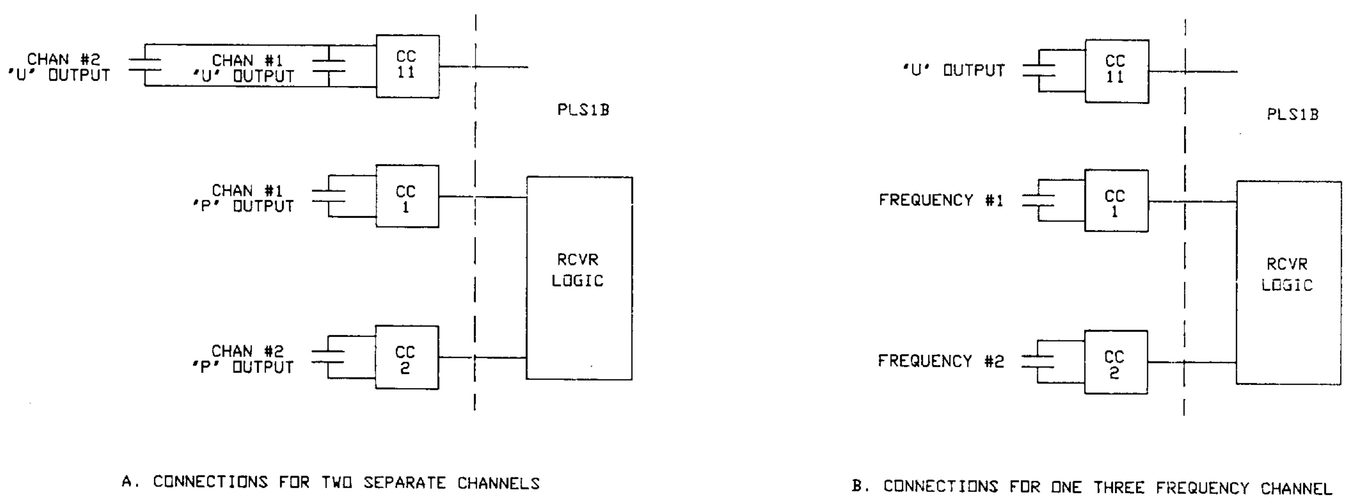


Figure SD-8 (0179C7549 Sh.4) Keying Circuits for Phase-Identified Channels



RECEIVER LOGIC



CHANNEL RECEIVER CONNECTIONS TO PLS1B

Figure SD-9 (0179C7549 Sh.5) Receiver Logic and Conections

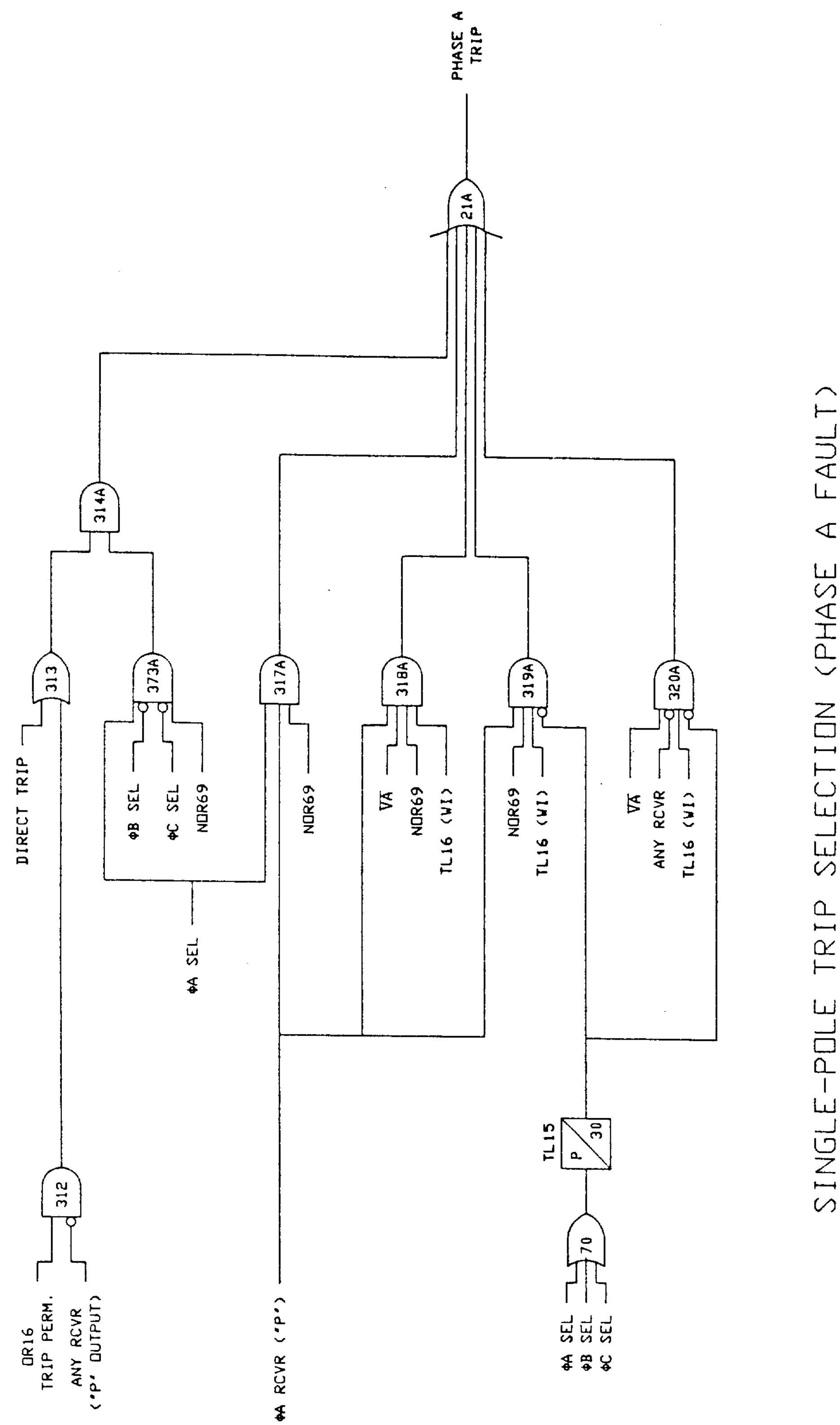


Figure SD-10 (0179C7549 Sh.6) Phase-A Trip Selection

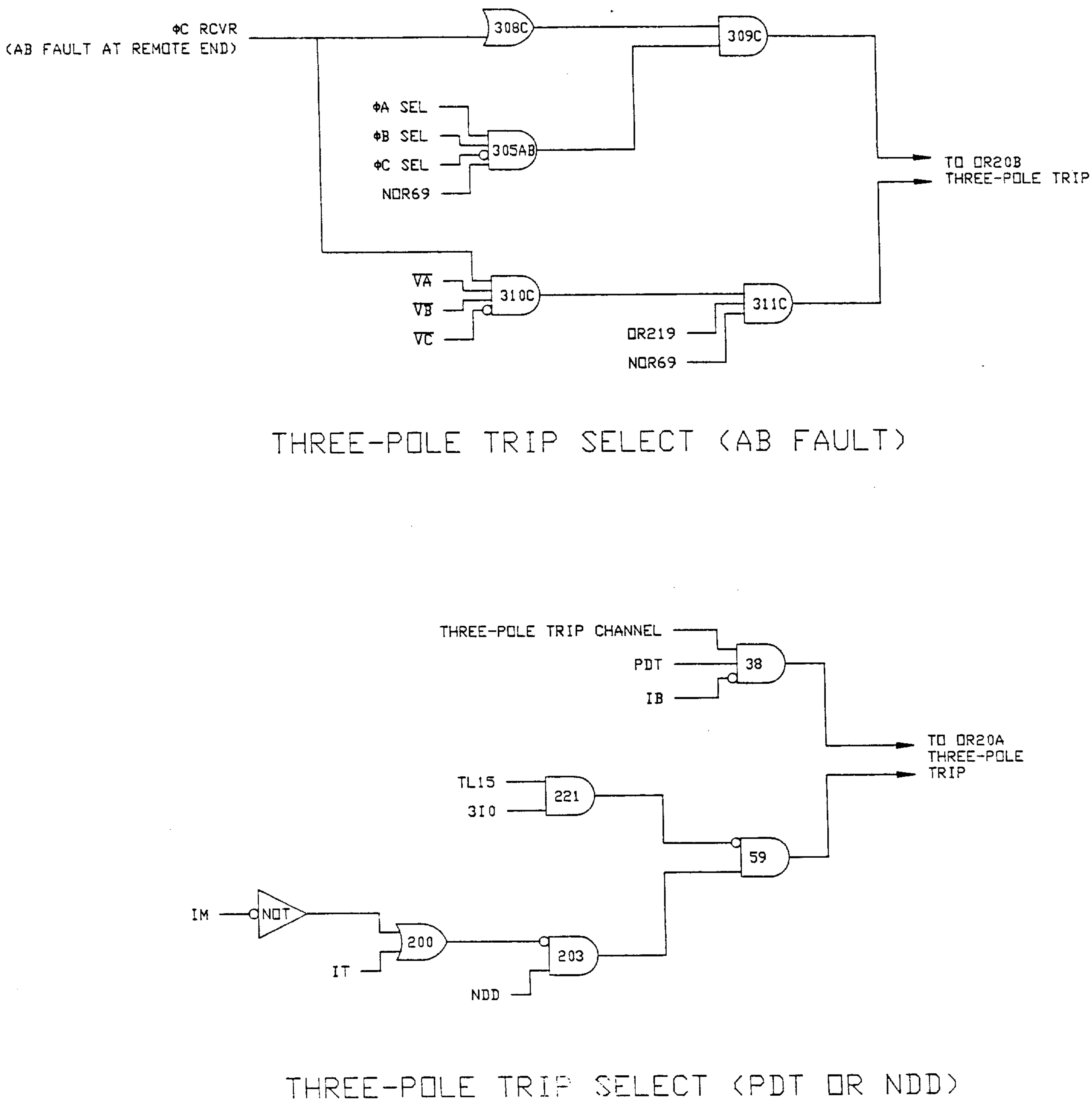


Figure SD-11 (0179C7549 Sh.7) Three-Pole Trip Selection

Calculation of Settings

CALCULATION OF SETTINGS

This section addresses the use of the PLS system on a two-terminal series compensated transmission line, and covers all of the required settings. The scheme is designed to be used with a single frequency shift (FSK) channel. Where the term line-side or Bus-side is used, it refers to the location of the potential source with respect to the series capacitor. See Figure 2 below which shows an example of line-side potential sources.

The designation for each setting as it appears on the respective module is indicated by underlining (e.g., ZR1). The module on which the setting is to be made is given in boldface (e.g. **AEM11-**).

PD1 AND ND - ZONE 1 DIRECT TRIPPING FUNCTIONS

The system is provided with positive sequence (PD1) and negative sequence (ND) direct tripping functions. They are used as straight distance functions on uncompensated lines, and must be used as a combined overcurrent/distance function when applied on series compensated lines, or on lines adjacent to compensated lines.

When applied as a straight distance function, the measurement is made by comparing the phase relationship of the operate signal (IZ-V) to a polarizing signal Vp; where Z is the reach of the function, and, V and I are the voltage and current at the function. In the combined mode of operation, the operate signal must also be larger than a user set magnitude in addition to having the correct relationship to the polarizing quantity. For example consider the fault at F in the system shown in Figure CS-1.

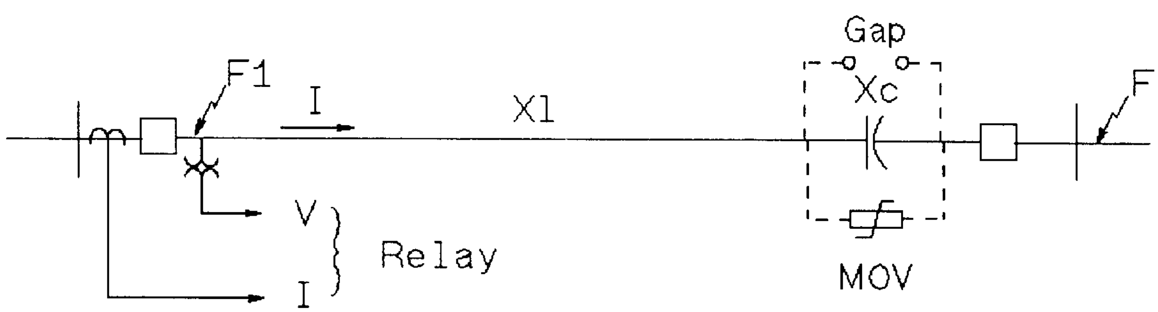


Figure CS-1 Sample Power System with Series Capacitors

On the surface, it appears feasible to set a straight distance function to reach 80-90 percent of the compensated impedance of the line (Xl-Xc) to provide direct tripping. However, the function may overreach on the low frequency transients that could occur for faults beyond the capacitor if the fault level is insufficient to cause gap flashing or significant conduction in the MOV's. Studies have shown that it may not be possible to set a straight distance function with a short enough reach to prevent overreaching. It is for this reason that the combined overcurrent/distance function was developed. The level detector setting is related to the amount of compensation and type of protection used around the compensation. For the fault at F, the voltage at the relay (R) is:

$$V = I(Xl - Xt)$$

Where:

Xt = Xc when gaps are used

Xt = parallel combination of Xc and MOV when MOV's are used

If the zone 1 function is set with a reach, Z, equal to Xl, then the operate signal (IZ-V) for the fault at F is:

$$IZ - V = I(Xl) - I(Xl-Xt) = I(Xl) - I(Xl) + I(Xt) = I(Xt)$$

If gap flashing does not occur, of if there is not significant conduction in the MOV, then the operate signal, IZ-V, is equal to I(Xc), the voltage across the capacitor. The level detector in the zone 1 function is set larger than this value so that it will not operate for faults external to the zone of protection, even in the presence of low frequency transients.

If, for the fault at F, the gaps flash or significant conduction occurs, then I*Xt is equal to the MOV protective level, or zero if the gaps flash. Because IZ - V is less than the level detector setting, the function is very secure for this condition.

Now consider a fault at F1 directly in front of the function. For this fault (V = 0), and the operate signal IZ-V = I(Z) = I(Xl). If the source behind the function is very strong and the line is very long, the operate signal will be very large and fast operation will result.

Settings

The following settings must be made:

Z1	**DPM11-**
PD1 Bias	**DPM11-**
ND Bias	**DNM10-**

In determining the level detector settings, it is necessary to consider external faults beyond any capacitor located at the buses in adjacent line sections. All of the capacitors that appear between the source of the relay potential and those external faults must then be taken into consideration. Consider the forward fault at location F2 in Figure CS-2:

1. Capacitors C1 and C2 need only be considered if line side potential is used.
2. If bus side potential is used then capacitor C, C1 and C2 must be taken into consideration.

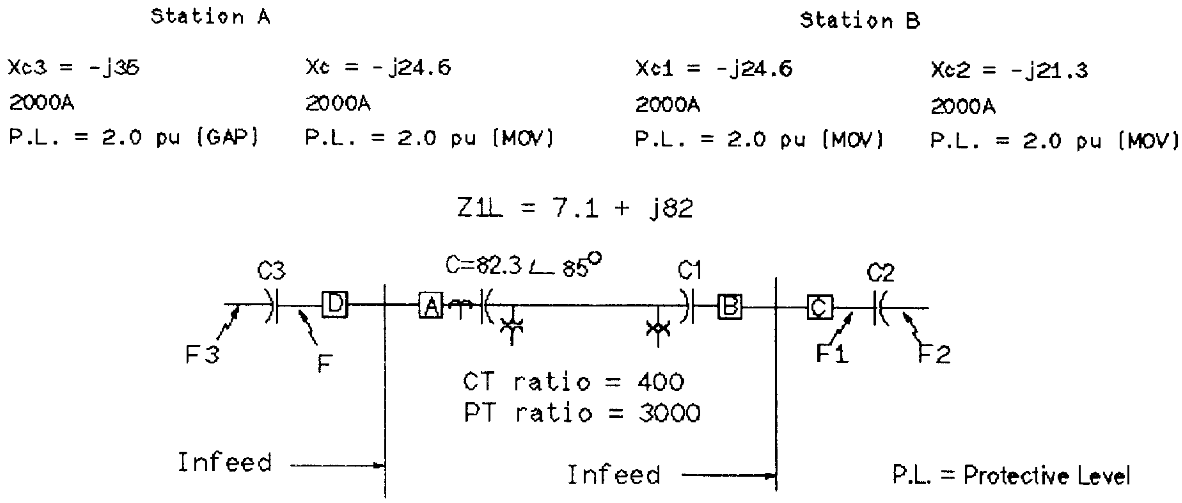


Figure CS-2 Sample Power System with Series Capacitors

Capacitor C2 should be treated as follows when determining the level detector settings:

1. With gaps: If the minimum fault current (I) for a fault at F1 is above the gap flashing level, then exclude C2 from the calculation.

2. With MOV's: If the MOV's are protected with gaps, and if the minimum fault current (including infeed) for a fault at F1 is above the gap flashing level, then exclude C2 from the calculation.

   If gaps are not used around the MOV's, or if the minimum fault current for a fault at F1 is below the gap flashing level, calculate an effective protective level as follows:

$$EP = \frac{(PL)(IPL)}{(I)} \tag{1}$$

Where: EP = effective protective level

PL = actual protective level in peak volts

IPL = rms current required to start conduction in the MOV's

I = minimum fault current for fault at F1

Note: Use the actual protective level (PL) if I is less than IPL

After it has been decided which capacitors should be considered, it is then necessary to sum the protective levels of those capacitors.

A. For series capacitors with protective gaps, the protective level is equal to the rms gap flashing level expressed in peak volts.

B. For capacitors with MOV protection, the protective level is established by the MOV's, and it is equal to the peak voltage allowed across the individual capacitor bank.

For the reverse fault at location F3 in Figure CS-2:

1. Capacitors C and C3 need to be considered if line side potential is used.
2. If bus side potential is used then capacitor C3 need only be taken into consideration.

Follow the same general rules given above when determining the effect of capacitor C3, except study a fault at location F.

PD1 Bias

The PD1 level detector setting (PD1 BIAS) is then equal to the sum of the protective levels divided by the peak phase-to-ground relay nominal design voltage [$\sqrt{2}(67)$ volts].

$$\text{PD1 Bias} = \frac{Vpt}{(\sqrt{2})(\text{PT ratio})(67)} \qquad (2)$$

Where:

Vpt = sum of protective levels of all involved capacitors (in primary volts)

ND Bias

The ND level detector setting (ND BIAS) is equal to 115 percent of the PD1 BIAS.

$$\text{ND Bias} = 1.15(\text{PD1 Bias}) \qquad (3)$$

Z1

The reach of the PD1 and ND functions is set via the Z1 setting. For lines with or adjacent to series capacitors, set Z1 equal to the positive sequence line impedance.

$$Z1 = \frac{Z1L(\text{CT ratio})}{(\text{PT ratio})} \qquad (4)$$

Where:

Z1L = positive sequence line impedance in primary ohms

NEGATIVE SEQUENCE DISTANCE REACH MULTIPLIERS, N2 AND N3

The ND function described above is used to provide high speed direct tripping and utilizes the **ND BIAS** setting to provide security in the presence of series capacitors. Another negative sequence distance function, designated NDD is used to provide the permissive function in the pilot portion of the scheme, and the backup function in the time-delayed portion of the scheme. NDD is initially set with the same reach, Z1, as the ND function, and is stepped out in reach as follows:

1. The NDD reach is extended to N2(Z1) when timer TL2 times out, or when both NT <u>and</u> IT have operated and a permissive trip signal is received from the remote terminal of the transmission line. Second zone backup tripping and/or pilot tripping is thus provided via the N2 setting.

2. The NDD reach is extended to N3(Z1) when timer TL3 times out. Third zone backup tripping is thus provided via the N3 setting.

It is proposed that the zone 2 reach [N2(Z1)] be set equal to the PDT reach to optimize performance for internal faults. However, if the function must coordinate with similar functions in adjacent line sections, then conventional zone 2 reach settings can be selected.

Set the zone 3 reach [N3(Z1)] to provide the required protection. If third zone protection is not required, set N3 = N2, and set timer TL3 greater than or equal to TL2.

Note that the ND function will also be extended in reach along with NDD, but will not provide the same zone of protection as NDD because of the ND BIAS setting which causes a pullback in reach.

Setting Example

The system shown in Figure CS-2 will be used.

Assumptions:

a. Pt ratio = 3000, CT ratio = 400

b. Infeed at Station A is sufficient to always cause flashing of the gaps around capacitor C3, therefore it can be ignored in determining the settings.

c. Infeed at Station B is insufficient to cause the fault current for a fault at F1 to exceed the level (IPL) at which conduction starts in the MOV around capacitor C2. Therefore, capacitor C2 must be taken into account in determining the settings.

d. The maximum peak voltage (2.0 p.u.) across the MOV protected capacitors is:

$$Vpcn = (2.0\ \text{p.u.})(Ic)(Xcn)$$

Where:

Ic = continuous rating (2000A in this example)

Xcn = reactance of respective capacitor

Vpcn = peak voltage across respective capacitor

Reach Setting, Z1

From equation (4) above,

$$Z1 = \frac{Z1L(\text{CT ratio})}{(\text{PT ratio})}$$

$$= \frac{82.3(400)}{3000}$$

$$= 10.97\Omega, \text{ use } 11\Omega$$

PD1 and ND Bias

Forward faults (must sum the voltages across C1 and C2):

$$Vpc1 = 2(2000)24.6 = 98400$$

$$Vpc2 = 2(2000)21.3 = 85200$$

$$Vpt = Vpc1 + Vpc2 = 183600$$

From equation (2), the PD1 setting, in per unit on a secondary base is:

$$\text{PD1 Bias} = \frac{183600}{\sqrt{2}(3000)67}$$

$$= 0.62 \text{ per unit, use } 0.63$$

From equation (3),

$$\text{ND Bias} = 1.15(\text{PD1 Bias})$$

$$= 1.15(0.63)$$

$$= 0.72, \text{ use } 0.74$$

Reverse Faults (must sum protective level across C alone)

Since capacitor C alone is involved, the total voltage will be less than that calculated for the forward fault, therefore the settings calculated above should be used.

PDT - POSITIVE SEQUENCE OVERREACHING DISTANCE FUNCTION

PDT is used as the overreaching function in the directional comparison portion of the scheme and is intended to operate for all three-phase faults and some double-line-to-ground (DLG) faults. PDT is also used in conjunction with the reclosing circuits, and in the phase selection circuits.

The PDT function is provided with zero sequence current restraint to prevent it from operating for close-in single-line-to-ground (SLG) faults. The restraint input is related to the reach (Z1) of the PD1 function plus a fixed factor of 30/In ohms; i.e.,

$$I0Zrest \approx (Z1 + 30/In)I0$$

The performance of the PDT function will be affected by this input. When longer than the proposed settings are used, the restraint becomes less effective and vice versa when shorter than proposed settings are used. Thus, when reach settings longer than the proposed settings are used, the function will operate for more DLG faults, but it will also be more prone to operation on close-in SLG faults. It is suggested that settings other than the proposed not be used on the PDT function when single-phase tripping is being utilized. If single-phase tripping is not being used, longer or shorter than the proposed settings may be used if desired. If reach settings shorter than proposed are used, PDT will operate for fewer DLG faults, plus it will also be slower in operation for these faults.

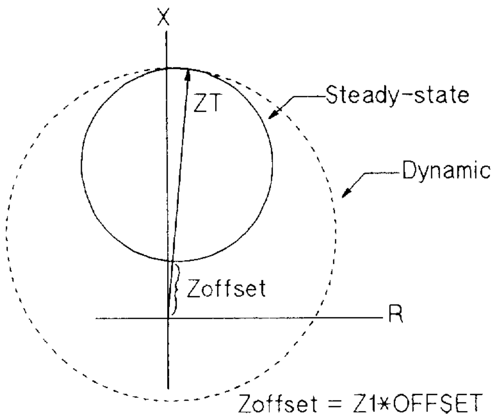


Figure CS-3 PDT Function

The PDT function can be set with a forward offset as shown in Figure CS-3 to the left, and the response of the function can be controlled via a time constant setting. Both of these features are used to minimize the effects of load flow.

Settings

The following settings must be made:

ZT	**DPM10-**
OFFSET	**DPM10-**
PDT TC	**DPM10-**

ZT - Forward Reach

The following setting is proposed:

$$ZT = \frac{Z1L(CT\ ratio)}{(PT\ ratio)} + \frac{30}{In} \qquad (5)$$

Where:

Z1L = uncompensated positive sequence impedance of transmission line
In = relay rated current (1A or 5A)

OFFSET - PDT Forward Offset

1. With line-side potentials:

   Use the following setting:

   OFFSET = 0.3

2. With bus-side potentials:

   Use the following setting:

   OFFSET = 0.2

PDT TC - PDT Time Constant

Use the following setting:

PDT TC = LONG

Setting Example

The system shown in Figure CS-2 will be used to demonstrate the settings for the PDT function at Station A.

Z1L = 11 ohms

From equation (5),

ZT = Z1L + 30/In = 11 + 6 = 17 ohms, use 17 ohms

OFFSET = 0.3

PDT TC = LONG

PDB - POSITIVE SEQUENCE DISTANCE BLOCKING FUNCTION

PDB is a positive sequence distance function that is used to provide one of the blocking functions that is required in the directional comparison portion of the scheme. The function is used in the weak-infeed and echo circuits, and in the transient blocking circuits.

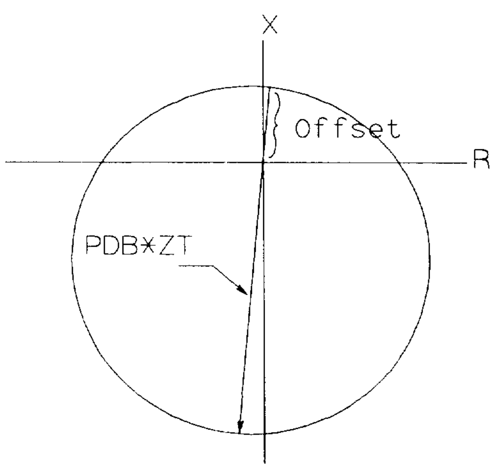


Figure CS-4 PDB Function

The blocking function has the characteristic shape shown to the left in Figure CS-4. The offset is equal to the forward offset in the PDT function and the reach of the function is a multiple (PDB) of the forward reach (ZT) of the PDT function (see Figure CS-3).

The PDB function also has a time constant setting that is used to control the response of the function.

Settings

The following settings must be made:

<u>PDB</u> **DPM10-**
<u>PDB TC</u> **DPM10-**

PDB - Reach

The reach of the PDB function is equal to the reach of the PDT function (ZT) multiplied by the blocking function reach multiplier, PDB [PDB reach = ZT(PDB)]. The following settings are proposed:

With line-side potentials or bus-side potential:

Calculate the following factor:

$$PDB1 = \frac{IL(ZT')}{67} \qquad (6)$$

a. If PDB1 ≤ 1.25 then

$$PDB = \frac{1.25}{PDB1} \qquad (7)$$

b. If 1.25 < PDB1 ≤ 1.5 then

$$PDB = \frac{1.5}{PDB1} \qquad (8)$$

c. If 1.5 < PDB1 ≤ 1.75 then

$$PDB = \frac{1.75}{PDB1} \qquad (9)$$

Where:

ZT' is the reach of the PDT function at the remote terminal of the transmission line.

IL is the maximum load current.

Use the next higher setting for PDB if an exact setting cannot be obtained.

PDB TC - PDB Time Constant

Use the following after first calculating PDB1 using (6) above:

PDB TC = SHORT, if PDB1 ≤ 1.5 (10)

PDB TC = LONG, if PDB1 > 1.5 (11)

PDB Setting Example

The system of Figure CS-2 will be used to demonstrate the settings for the PDB functions at Station B.

ZT' at Station A = 17

ZT = 17 at Station B

IL = 4.8 amperes (maximum load current)

PDB1 = $\frac{4.8(17)}{67}$ = 1.2, therefore, from equation (7),

PDB = $\frac{1.25}{1.2}$ = 1.04

Use a PDB setting of 1.25

PDB TC = SHORT (PDB1 $<$ 1.5)

POSB - POSITIVE SEQUENCE OUT OF STEP DISTANCE FUNCTION

POSB is a positive sequence distance function that works in conjunction with the PDT function to establish out-of-step blocking. The reach of POSB is equal to POSB*ZT where POSB is a reach multiplier and ZT is the reach set on the PDT function. The POSB function also has a time constant setting that is used to control the response of the function.

The following settings must be made:

POSB	**DPM10-**
POSB TC	**DPM10-**

POSB - Reach Multiplier

Use the following setting:

POSB = 1.1

POSB TC - Time Constant

Set POSB TC equal to the setting selected for PDT TC.

PDX - POSITIVE SEQUENCE AUXILIARY DISTANCE FUNCTION

PDX is a positive sequence distance function that is used to control timer TL2 to provide time-delayed backup protection, and it is also used in the reclosing circuits.

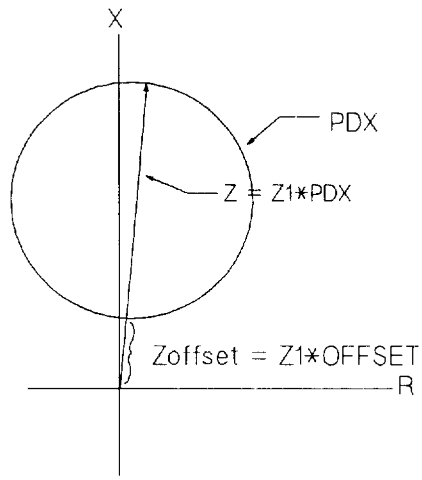


Figure CS-5 PDX Function

PDX has the characteristic shown in Figure CS-5 to the left. The reach of PDX is equal to PDX(Z1) where PDX is a reach multiplier and Z1 is the reach of the PD1 and ND functions.

The following setting must be made:

<u>PDX</u> **AEM10-**

Select a reach [PDX(Z1)] to provide coordination with similar functions in adjacent line sections, or to meet reclosing control requirements as described in a later section of this book.

ZR1 - SYSTEM IMPEDANCE ANGLE

The ZR1 setting sets the impedance angle for all of the distance functions.

The following setting must be made:

<u>ZR1</u> **AEM11-**

ZR1 must be set equal to, or just below, the positive sequence impedance angle of the transmission line.

Setting Example

See Figure CS-2.

ZR1 = 85°

NT AND NB - NEGATIVE SEQUENCE DIRECTIONAL FUNCTIONS

Settings

The following settings must be made:

<u>KT</u> **ADM10-**
<u>VA2</u> **AEM11-**

KT

The negative sequence directional tripping function (NT) uses an "offset" or compensating signal in the operating quantity to provide a dependable operating signal when the function is applied on a series compensated line. Consider the system shown in Figure CS-6 below.

Line-Side Potential

For the fault shown, and with line-side potential, the negative sequence voltage at the relay will be reversed from normal if the fault current is not sufficient to cause flashing of protective gaps, or significant conduction in MOV's. If this voltage alone was used in a negative sequence directional function, it would produce an erroneous output in that the fault would appear to be external to the line rather than internal to the line as shown in the figure. The operate signal for the NT function is:

NT(operate) = V2 - (1 + KT)(I2)Z

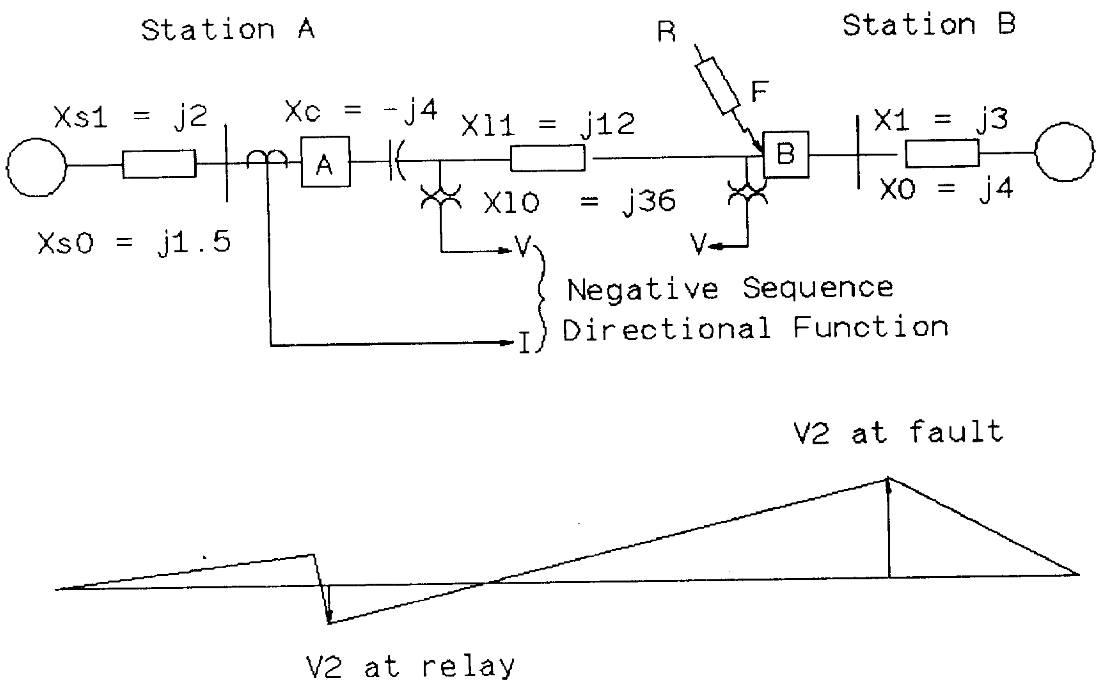


Figure CS-6 Negative Sequence Network and Voltage Profile

Where:

V2 = negative sequence voltage at relay

I2 = negative sequence current at relay

KT = offset factor

Z = NT offset reach

Determination of the offset factor is related to the offset reach (Z) of the NT function and the size of the series capacitor located between the potential source and the adjacent bus (Xc in Figure CS-6). The offset reach is fixed at 100/In ohms (In = 1A or 5A) and KT is adjustable from 0 to 1. KT is calculated as follows:

$$KT = \frac{(1.1)(2)(Xc)(In)}{100} = (0.022)(Xc)(In) \qquad (12)$$

Where:

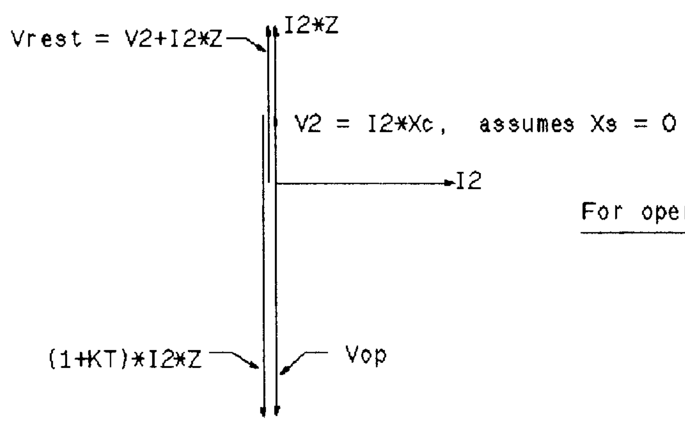
Xc = capacitive reactance of capacitor located between bus and source of potential (in secondary ohms)

In = relay rating, 1A or 5A

The derivation of KT is given in Figure CS-7 which applies for a single-line-to-ground at F in Figure CS-6. Operation will be similar for the other types of unbalanced faults.

For conditions shown: Vop = (1+KT)*I2*Z - V2

Vrest = V2+I2*Z



For operation: Vop > Vrest

(1+KT)*I2*Z - V2 > V2+I2*Z

KT*I2*Z > 2*V2

KT > (2*V2)/(I2*Z)

KT > (2*I2*Xc)/(I2*Z)

KT > 2*Xc/Z

Z = 100/In, and applying a 10% margin:

KT = (1.1)*(2)*(Xc)*(In)/100

Figure CS-7 Derivation of KT

The sum of [KT(100/In)] for the settings at both ends of the line must not exceed 160 percent of the uncompensated, positive sequence line impedance. If the above calculation results in a sum that exceeds 160 percent, then the KT settings should be decreased proportionally at each end so that the sum is equal to or just below the maximum value.

NOTE: <u>If there are no capacitors located between the bus and the source of potential, such as at Station B in Figure CS-1, set KT = 0.05</u>.

BUS-SIDE POTENTIALS

When bus side potentials are used, the voltage will not reverse, even for a fault adjacent to the capacitor. The offset factor in this case is based on the compensated line impedance and is calculated as follows:

$$KT \leq (0.0055)(Z2L - Xct)(In) \qquad (13)$$

Where:

Z2L = negative sequence line impedance (in secondary ohms)

Xct = total series capacitance appearing between the potential sources located at each end of the line (in secondary ohms)

Use the same KT setting at each end of the line.

VA2

The VA2 setting introduces a phase shift in the negative sequence voltage quantity (V2) used in the negative sequence directional functions. VA2 is calculated as follows:

VA2 = (85° - ZSang)

Where:

ZSang = the angle of the effective source impedance behind the relay.

If ZSang is greater than or equal to 80°, set VA2 = 0.

Setting Example

The system shown in Figure CS-6 will be used in determining the settings for the negative sequence directional functions at both line ends.

Station A

From equation (12)

KT = (0.022)(4)(5) = 0.44

Use a setting of 0.45

VA2 = 0, since ZSang > 80°

Station B

KT = 0.05, since no capacitors located between bus and source of potential

VA2 = 0 since ZSang >80°

Check that sum of KT*100/In at both line ends is less than 160 percent of uncompensated positive sequence line impedance.

$$(0.45+.05)(100/5) < 1.6(12)$$

$$10 < 19.2$$

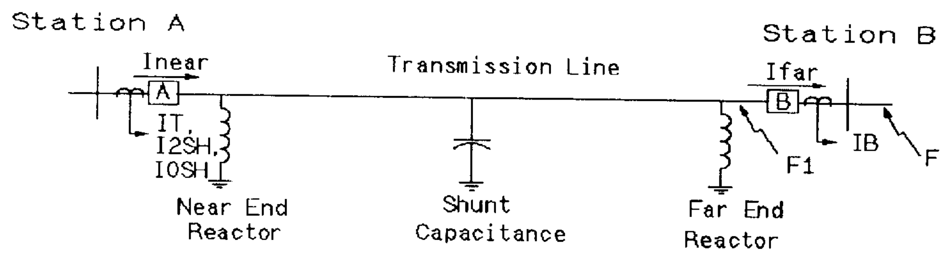
Application is okay with settings calculated above.

IT, IB, I2 SHUNT AND I0 SHUNT

The IT (tripping) and IB (blocking) functions are used in the directional comparison scheme along with the negative sequence directional functions to provide sensitive tripping for ground faults. The following operating signals are used:

$$\text{IT operate signal} = (2|I0| + |I2| - 0.3|I1|)$$
$$\text{IB operate signal} = (2|I0| + |I2| - 0.2|I1|)$$

IT and IB must coordinate with each other. This coordination is achieved via the settings placed on the functions, with the requirement that IB at one terminal of the line be more sensitive than IT at the other terminal. For example, IB at Station B in Figure CS-8 below must be more sensitive than IT at station A.



Transmission Line:
- XL2 = negative sequence reactance
- XL0 = zero sequence reactance

Far End Reactor:
- XRF2 = negative sequence reactance
- XRF0 = zero sequence reacxtance

Near End Reactor:
- XRN2 = negative sequence reactance
- XRN0 = zero sequence reactance

Shunt Capacitance:
- XC2 = negative sequence reactance
- XC0 = zero sequence reactance

Figure CS-8 Sample Power System

Note that the negative and zero sequence currents entering the line will be greater than the respective currents leaving because of the charging current. This must be taken into account. In Figure CS-8 for example, the negative and zero sequence currents at Station A (Inear) will be greater than the respective current at Station B (Ifar). How much the current will differ will be affected by any shunt compensation used on the line (such as the far end and near end reactors shown in the figure). It is possible to compensate for the effect of the charging current by simply setting IT greater than IB by the amount of the charging current. However, this would entail a fixed difference in setting which would fix the sensitivity of IT. To overcome this limitation, the IT function is provided with an adaptive restraint via the I2 SHUNT and the I0 SHUNT inputs. For example, for a phase-to-phase fault at F in Figure CS-8, the negative sequence voltage will be relatively large, which in turn will produce a large restraining quantity which is desirable in this instance to assure positive coordination. On the other hand, consider a high resistance fault at F1. For this condition, the negative and zero sequence voltages will be quite low, thus the restraining effect of I2 SHUNT and I0 SHUNT on the IT function at Station A will be minimized thus allowing greater sensitivity for resistive faults.

Settings

The following settings must be made (see Figure CS-8 for definition of parameters):

<u>IB BIAS</u>	**ADM10-**
<u>IT BIAS</u>	**ADM10-**
<u>I2 SHUNT</u>	**ADM10-**
<u>I0 SHUNT</u>	**ADM10-**

IB Setting (IB Bias)

Set the IB function to its minimum setting of 0.05 per unit regardless of where the potential source is located.

IT Setting (IT Bias)

1. With line-side potential

$$IT\ Bias = [IB + 0.025 + 0.1(I1SH)]K1 \qquad (15)$$

Where:

$$K1 = [1 + \frac{0.75(XL2)}{XC2} + \frac{1.5(XL0)}{XC0} - \frac{XL2}{XRF2} - \frac{2(XL0)}{XRF0}] \qquad (16)$$

$$I1SH = \frac{67}{XC1(In)} \qquad (17)$$

IB = IB Bias setting at remote end of line

NOTE: If there are no far end reactors (XRF2 and XRF0 = infinity) the last two terms in (16) go to zero

IT Bias SHOULD NEVER BE SET LESS THAN 0.1

I2 SHUNT Setting (I2 SHUNT)

$$I2\ SHUNT = \frac{(XRN2 - X2)67}{XRN2(X2)In} \qquad (18)$$

NOTE: If there are no near end reactors (XRN2 = infinity), thus,

$$I2\ SHUNT = \frac{67}{X2(In)} \qquad (19)$$

Where:

$$X2 = \frac{XC2[(0.25)XL2 + XRF2]}{XRF2 + 0.25(XL2) - XC2} - 0.75(XL2) \qquad (20)$$

NOTE: If there are no far end reactors (XRF2 = infinity), thus,

$$X2 = XC2 - 0.75(XL2) \qquad (21)$$

I0 SHUNT Setting (I0 SHUNT)

$$I0\ SHUNT = \frac{(XRN0 - X0)134}{XRN0(X0)In} \qquad (22)$$

NOTE: If there are no near end reactors (XRN0 = infinity), thus,

$$I0\ SHUNT = \frac{134}{X0(In)} \qquad (23)$$

Where:

$$X0 = \frac{XC0[(0.25)XL0 + XRF0]}{XRF0 + 0.25(XL0) - XC0} - 0.75(XL0) \tag{24}$$

NOTE: If there are no far end reactors (XRF0 = infinity), thus,

$$X0 = XC0 - 0.75(XL0) \tag{25}$$

2. With bus-side potential

When bus-side potential is used, bypassing of one or two phases of the capacitor bank could cause the related unbalance (due to load) to appear as an internal fault to the negative sequence directional functions. To prevent tripping, the IT function must be set above the unbalanced current produced during this condition. The following procedure is suggested:

1. Calculate the IT BIAS setting as described above.
2. Determine the value of IT(operate) that is produced with maximum load flowing and with one or two phases of the capacitor bank bypassed; i.e., find

   $$IT(operate) = [2|I0| + |I2| - 0.3|I1|]/In$$

3. Compare this value with the IT BIAS setting obtained in 1 above. If IT(operate) is greater than the setting so calculated, then increase the IT BIAS setting accordingly.

Setting Example

The IT BIAS, IB BIAS, I2 SHUNT and I0 SHUNT settings described below pertain to the IT function at Station A and the IB function at Station B. Except where noted otherwise, all of the factors used in the equations are described in Figure CS-8. All reactance values must be expressed in secondary quantities. The settings will all be determined in per unit where the base current, In (1.0 or 5.0 amperes), is the relay rated current. The following values (in secondary terms) apply.

Transmission Line	Near End Reactor (none)	Far End Reactor
XL2 = 14.1	XRN2 = ∞	XRF2 = 204
XL0 = 52.5	XRN0 = ∞	XRF0 = 204
XC1 = XC2 = 104		
XC0 = 156		

IT Bias

From equation (17),

$$I1SH = \frac{67}{104(5)} = 0.129$$

From equation (16),

$$K1 = [1 + \frac{0.75(14.1)}{104} + \frac{1.5(52.5)}{156} - \frac{14.1}{204} - \frac{2(52.5)}{204}] = 1.022$$

From equation (15),

$$IT\ BIAS = [0.05 + 0.025 + 0.1(0.129)]1.022 = 0.09$$

Since this is less than 0.1, use the minimum recommended setting of 0.1.

I2 SHUNT

Since there are no near end reactors, use equation (19) above after first calculating X2 using equation (20).

$$X2 = \frac{104[(0.25)14.1 + 204]}{204 + 0.25(14.1) - 104} - 0.75(14.1) = 197.9$$

$$I2\ SHUNT = \frac{67}{197.9(5)} = 0.068$$

Use a setting of 0.07

I0 SHUNT

Since there are no near end reactors, use equation (23) above after first calculating X0 using equation (24).

$$X0 = \frac{156[(0.25)52.5 + 204]}{204 + 0.25(52.5) - 156} - 0.75(52.5) = 514.8$$

$$I0\ SHUNT = \frac{134}{5(514.8)} = 0.052$$

Use a setting of 0.05

IDT - OVERCURRENT DIRECT TRIPPING FUNCTION

The IDT direct tripping overcurrent function uses zero sequence current and may be applied with or without positive sequence current restraint. The IDT operating quantity is:

$$IDT(operate) = (3|I0| - K1|I1|) \quad (26)$$

Where:

$K1 = 1$ or 0

Positive sequence current restraint is recommended ($K1 = 1$) because it makes the function less sensitive to external faults, while providing excellent sensitivity for close-in internal faults.

For example, with $K1 = 1$, consider the following three cases for the system shown in Figure 9.

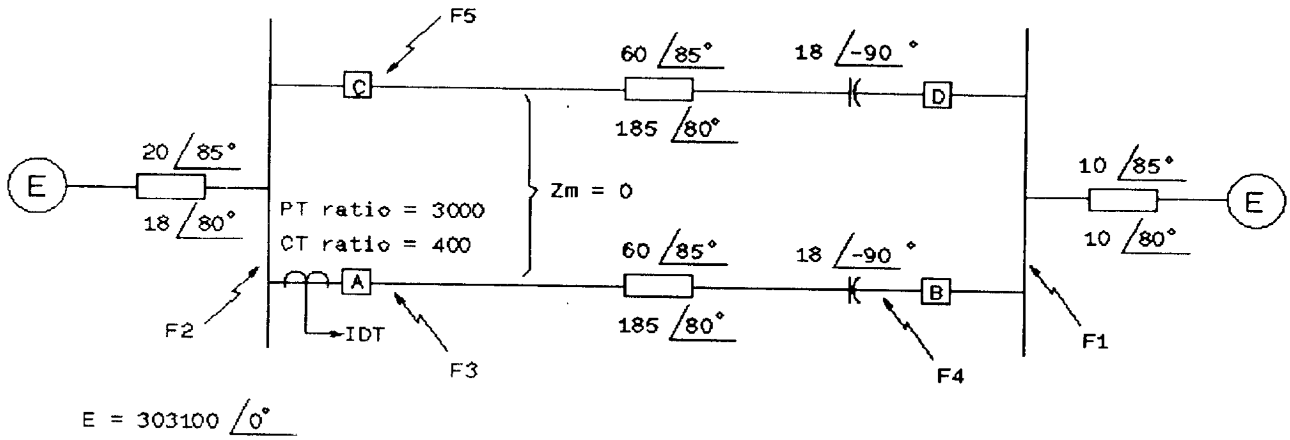


Figure CS-9 Sample Power System

Case 1, SLG fault at F1, all breakers closed

I1 = 1180A I0 = 540A

IDT(operate) = [3(540) - 1180] = **440A**

Case 2, SLG fault at F4, breaker B open

I1 = 1023A I0 = 1023A

IDT(operate) = [3(1023) - 1023] = **2046A**

Case 3, SLG fault at F3, all breakers closed

I1 = 6187A I0 = 7073A

IDT(operate) = [3(7073) - 6187] = **15032A**

NOTE: If K1 is set to zero, the operating quantity is simply equal to three times (3x) the zero sequence current given above. This must be remembered in determining an appropriate IDT setting if positive sequence current restraint is not used.

Assume for this example that K1 = 1 and that the IDT function is set to pick up at 0.5 per unit amperes. For a 5 ampere rated relay, and for the CT ratio shown in Figure CS-1, this transposes to a pickup of 1000 primary amperes. The following can be noted:

1. The function will not operate for Case 1.
2. The function will operate for Case 2, but only after breaker B opens. This will be a sequential trip because operation of IDT follows the opening of breaker B.
3. The function will operate for Case 3. It will be very fast because the operating quantity is 15 times the pickup setting.

Another input is also applied to the energy comparator in addition to the operate signal described above. This signal which uses zero sequence current is effective for close-in heavy faults, and is used to speed up operation of IDT. This input is further described in the setting example provided below.

The IDT function can be directionally controlled by the negative sequence directional functions if desired. Directional control is best used in those applications where the maximum operating quantity that is developed for external faults directly behind the function is greater than the maximum operating quantity developed for external faults at the remote terminal. If the maximum operating quantities are approximately equal for external faults at each end of the line then directional control is not necessary, and its use may be detrimental. For example, consider a fault that occurs at F5 in Figure CS-9 and then evolves into an internal SLG fault at F3 that is sufficient to operate IDT. If directional control is used, then tripping at F3 cannot occur until the transient blocking time (established by reset time of blocking function) has elapsed. On the other hand, tripping will occur immediately if directional control is not used.

When using directional control, it is only necessary to evaluate the effects of faults just beyond the remote terminal in determining an appropriate setting. If directional control is not used, then it will be necessary to evaluate the effects of faults directly behind the function as well as at the remote terminal.

Settings

The following settings must be made:

IDT K1	**DPM11-**
K0	**DPM11-**
DT PU	**DPM11-**
IDT DIR	**DPM11-**

Setting Example

The system shown in Figure CS-9 will be used in this example.

IDT K1 - This setting (K1 = 0 or 1) establishes the amount of positive sequence current restrain that is used. Use the recommended setting of 1.

KO - This setting establishes the magnitude of the additional operate signal [K0(I0)ZR1] that is applied to the energy comparator to help speed up operation of IDT. KO is calculated as follows:

$$KO = \frac{(Z0L - Xc)K}{|Z1L|} \qquad (27)$$

Where:

Z0L = | zero sequence impedance of the protected line|

Z1L = | positive sequence impedance of the protected line|

Xc = | total capacitive reactance of any series capacitors in the line|

K = 1, if there is no mutual coupling with parallel lines

$$K = 1 - \frac{Zm^2}{(Zol - Xc)Zop} \qquad (28)$$

Where:

Zm = | zero sequence mutual impedance between protected line and parallel line|

Zop = | zero sequence impedance of parallel line|

NOTE: Use impedance magnitudes only in making the calculations, do not use phasor quantities.

For the system shown in Figure CS-9, and using equation (27):

$$K0 = \frac{(185 - 18)}{60} = 2.78$$

Use a setting of 2.8.

DT PU - The DT PU setting is established by determining the maximum positive value of:

$$IDT(operate) = (3|I0| - K1|I1|) \qquad (28)$$

If IDT is to be directionally controlled then the operate signal need only be evaluated for faults at F1. If IDT is not to be directionally controlled, then it will be necessary to evaluate the quantity for faults at F2 also. The IDT pickup setting (DT PU) is then equal to the maximum operate signal so determined plus a margin of 25% of the (3| I0|) used in determining the maximum value of the operate signal.

$$DT\ PU = (3|I0| - K1|I1|) + 0.25(3|I0|) \qquad (29)$$

TABLE CS-1 Fault Study of Figure CS-9

Case	Fault	Caps.	Line C-D	I1	3(I0)	Iop	Iop+0.25(3I0)
1	F2	Out	In	1204	1620	416	821
2	F1	Out	In	979	1461	482	847
3	F2	Out	Out	1417	1617	200	604
4	F1	Out	Out	1234	1566	332	723
5	F2	In	In	1507	1860	353	818
6	F1	In	In	1180	1617	437	841
7	F2	In	Out	1860	1854	(-6)	458
8	F1	In	Out	1575	1704	168	604

Table CS-1 lists the results of a fault study for faults at locations F1 and F2 as shown in Figure 9.

From this table it can be seen that the there is not a significant difference between the maximum Iop for a fault at F1 (482) versus the maximum Iop for a fault at F2 (416). On this basis, the function can be operated without directional control. It should be set to pickup at 847 primary amperes.

$$DT\ PU = \frac{847}{CT(In)} = \frac{847}{400(5)} = 0.42 \text{ p.u.}$$

Use a setting of 0.5 p.u.

Set the IDT DIR control jumper to the NON-DIR position.

I1T - POSITIVE SEQUENCE OVERCURRENT LINE PICKUP FUNCTION

The I1T function operates from positive sequence current and is provided for use in the line pickup (close-into-fault) circuit.

I1T should be set to pick up at no greater than 2/3 of the minimum fault current for an internal three-phase fault on the line at a point equal to the forward offset setting [e.g. Zfault = OFFSET(ZT)].

If the minimum fault current is greater than the maximum load current across the line, the I1 setting can be reduced to provide greater coverage of the line. For this case, a setting of 110% of the maximum load current is proposed. If the I1T function can be set with a pickup of at least 110% of the maximum load current contact converter CC6 can be energized continuously to bypass coordinating timer TL8 to obtain faster tripping.

If sequential reclosing is used, or if there is no automatic reclosing, then I1T can be set below load current, and CC6 can be energized continuously to bypass timer TL8. If high-speed simultaneous reclosing is used and I1T is set below full-load current, then TL8 should be continuously energized, otherwise tripping might be initiated when picking up a loaded line.

If a power transformer is energized when the line is reclosed, CC6 should not be continuously energized to bypass TL8 if I1T can pick up on the transformer inrush current. A conservative approach to determine if I1T will pick up on the transformer inrush is to calculate the steady-state positive sequence current for a three-phase through fault just on the other side of the transformer; i.e., at the transformer bushings. If I1 will pick up for this fault, then TL8 should not be bypassed.

The following setting must be made:

<u>I1</u> **AEM1--**

Setting Example

The system shown in Figure CS-9 will be used in determining the setting for I1T at Station A.

For this line, ZT = 5.3 ohms, per equation (5), and OFFSET = 0.3 if line side potential is used.

The minimum three-phase fault current in per-unit for a fault at a point equal to the offset setting of 1.6 secondary ohms, or 18 primary ohms is:

$$\text{Imin} = \frac{303100}{400(38)5} = 4.0 \text{ per-unit amperes}$$

Assume further that the maximum load current across the line is 4.8 amperes. In per-unit, this is:

$$\frac{\text{Iload}}{5} = \frac{4.8}{5} = 0.96 \text{ per-unit amperes}$$

Since the minimum fault current is greater than the maximum load current, a setting based on 110 percent of the maximum load is proposed.

$$\text{I1} = 1.1(0.96) = 1.06, \text{ use a setting of } 1.2 \text{ per-unit}$$

ITOC - TIME OVERCURRENT FUNCTION

The ITOC very inverse time overcurrent function uses zero sequence current and may be applied with or without positive sequence current restraint. The function is used to provide time-delayed backup tripping for faults involving ground. It uses the following operating quantity:

$$ITOC(operate) = 3|I0| - K1|I1| \quad (30)$$

Where: K1 = 0 or 0.45

Positive sequence current restraint is used to make the function less sensitive to external ground faults. In selecting the settings for ITOC, consideration should be give to:

a. Coordination with other ITOC functions in adjacent lines

b. Coordination with conventional ground TOC functions on adjacent lines

c. Coordination with the zero sequence current produced as a result of an open pole in an adjacent line section

If coordination with conventional ground TOC functions is required, then the suggested approach is to calculate the pickup and time dial settings assuming no positive sequence restraint, but to then use positive sequence restraint in the application. The use of this restraint will provide an additional coordinating margin for ITOC and increase security by preventing undesired operation due to zero sequence error current resulting from load flow over untransposed lines, unsymmetrical gap flashing across series capacitors.

The ITOC function can be directionally controlled by the negative sequence directional functions if so desired. Directional control should be considered if it becomes difficult to coordinate the ITOC function with similar functions in adjacent line sections.

The following settings must be made:

TOC PU	**DPM11-**
TOC K1	**DPM11-**
TD	**DPM11-**
TOC DIR	**DPM11-**

TOC PU

TOC PU determines the pick up setting and is set in per-unit on the relay rated ampere base (In = 1A or 5A):

$$TOC\ PU = \frac{ITOC(operate)}{In} \quad (31)$$

Use equation (30) to calculate the minimum ITOC(operate) for which the ITOC function must operate.

TOC K1

TOC K1 is used to remove (TOC K1 = 0) positive sequence restraint, or to apply (TOC K1 = 0.45) positive sequence restrain. Select the appropriate setting to meet the application.

TOC DIR

TOC DIR selects whether or not the function will be directionally controlled by the negative sequence directional functions. Select the appropriate setting to meet the application.

TD

TD sets the time-dial setting for the ITOC function. Select an appropriate setting to meet the application.

IMA, IMB, IMC - PHASE CURRENT FUNCTIONS

The IM functions are used in the open-pole detector circuits and in the breaker failure (BFI) seal-in circuits.

The following setting must be made:

IM **AEM10-**

Use the following setting:

$$IM = \frac{1.5(I1c)}{In}$$

Where:

I1c = the net positive sequence charging current, taking into account any shunt reactors that are in service with the remote end of the line open

3I0 - ZERO SEQUENCE CURRENT FUNCTION

3I0 is used to provide supervision to the negative sequence distance functions to prevent them from initiating a three-pole trip during single-line-to-ground faults. The setting is made in per unit of the relay rated current, In = 1A or 5A.

The following setting must be made:

3I0 **AEM10-**

Use the following setting:

$$3I0 = \frac{I0x}{In}$$

Where, I0x equals the lower of:

1. 30 percent of the maximum load current, or
2. two-thirds (2/3) of the 3I0 current for a single-line-to-ground fault at the remote end of the transmission line.

OSB1, OSB2 - OUT-OF-STEP BLOCKING

Out-of-step blocking (OSB) is provided in the PLS system. Two switches are provided to route the OSB output to do the following in the logic:

OSB1

Set this switch to the in position to block zone 1 and pilot tripping, zone 2 and zone 3 time-delayed tripping, and to block all transmitter keying.

OSB2

Set this switch to the IN position to block all tripping, including those functions blocked by OSB1. Consideration should be given to setting the OSB2 switch to the IN position in those applications where the breaker is incapable of interrupting during an out-of-step condition.

LOGIC TIMERS

The following timers must be set:

ZONE 2	**ULM19-**
ZONE 3	**ULM19-**
WEAK INFEED	**ULM19-**
TL1	**ULM19-**
TL9	**ULM19-**
TL24	**ULM19-**
TL25	**ULM19-**
TL26	**ULM17-**

Zone 2

The ZONE 2 setting applies to timer TL2 in the logic and that is used with the PDX function to provide time-delayed backup tripping if desired. The timer may be switched out altogether if required. Select an appropriate setting for the application.

Zone 3

The ZONE 3 setting applies to timer TL3 in the logic and that is used with the PDT function to provide time-delayed backup tripping if desired. The timer may be switched out altogether if required. Select an appropriate setting for the application.

Weak Infeed

The WEAK INFEED setting applies to timer TL16 in the logic that is used to provide security against spurious receiver outputs causing false trips through the weak infeed logic. Use a WEAK INFEED setting of 5 milliseconds unless it is determined that spurious outputs could last longer in which case the timer setting should be increased accordingly.

TL1

The TL1 setting applies to timer TL1 in the logic that is used to provide security against spurious receiver outputs during external fault conditions. A minimum setting of 3 milliseconds is proposed if a GE Type 71 channel is used. Longer settings will be required if it is determined that the spurious outputs will last longer than 3 milliseconds.

TL9

The TL9 setting applies to timer TL9 in the logic that is used to supervise the channel repeat circuit. Use a TL9 setting of channel time minus 4 milliseconds.

TL24

The TL24 setting applies to timer TL24 in the logic that is used to establish the dropout time of the NB negative sequence blocking function. Use a TL24 setting of 120 milliseconds.

TL25

The TL25 setting applies to timer TL25 in the logic that is used to establish the dropout time of the PDB positive sequence blocking function. A minimum setting of 120 milliseconds is proposed.

However, the following must be considered (please refer to Figure CS-2). The PDB function on line A-B at station A will operate correctly on a dynamic basis for a three-phase fault at location F. PDB will block tripping of breaker A and will prevent repeat of the channel signal to Station B and so prevent tripping there. If, however, breaker D fails to clear normally, and if the gaps/MOV's across capacitor C have not flashed/conducted, then PDB could drop out and PDT could pick up as a result of the voltage reversal that occurs because of capacitor C. The 120 millisecond dropout time may then not be long to allow the breaker failure relaying at breaker D to time out to do the clearing before line A-B is tripped. If this is not acceptable, then it will be necessary to increase the TL25 setting beyond the breaker failure relaying time set at the breakers in adjacent line sections. Note that any increase in the TL25 setting will introduce added delays in tripping in the event an external fault would evolve into an internal fault on the line in which PDB is located.

TL26

The TL26 setting applies to timer TL26 in the logic that is associated with phase selector operation. Use a TL26 setting of the nominal breaker opening time minus a half-cycle (e.g., 25 milliseconds for a 2-cycle breaker on a 60 Hz system).

TL13, TL22- TRANSFER TRIP TIMERS

The following settings must be made:

TL13	**ULM15-**
TL22	**ULM15-**

Settings for these timers are required only if the output from the direct transferred trip receivers are routed to contact converter CC3 in the logic. If the PLS system is not used with these receivers, then these two timer settings have no effect and may be left set at any value. When transferred tripping is used, use a TL13 setting that is greater than the maximum spurious output expected from the transferred trip receivers.

Use a TL22 setting that will discriminate between a trip signal produced by a line fault as opposed to a transferred trip signal that is produced because of equipment fault (transformer, etc.) or a breaker failure. This discrimination is based on the duration of the transferred trip signal. Trip signals produced for a line fault will be relatively short and will be less than the TL22 setting thus preventing it from timing out. On the other hand, for equipment faults, or breaker failure, the transferred trip signal will be prolonged and will be greater than the TL22 setting. When timer TL22 times out it will energize the lockout reclosing relay (LR) in the PLS system, the output of which can be used to prevent reclosing.

RECLOSING CONTROL

The PLS system is provided with two outputs that can be used in the external reclosing control circuits.

1. Lockout Reclosing

The lockout reclosing (LR) output is always activated by any one of the following:

a. Direct Transferred Trip (timer TL22 output)

b. TL2 (zone 2 timer) output

c. TL3 (zone 3 timer) output

d. ITOC (time-delayed trip) output

e. CC8 (external trip input to logic) output

f. OSB AND any Trip Bus (trip during out-of-step)

The LR output, as its name implies, is used to lockout or block all reclosing because the inputs that are used to activate it generally indicate that a fault of a permanent nature has occurred. Reclosing can be blocked externally via the lockout reclosing contacts, or the reclose initiate (RI) functions provided in the PLS can be blocked internally via a switch (BLOCK RI) provided in the logic.

2. Inhibit Reclosing

The inhibit reclosing (IR) output may be activated by any one of the following:

a. PD1 output (zone 1 positive sequence direct trip)

b. ND output (zone 1 negative sequence direct trip)

c. PDX output (positive sequence direct trip)

d. PDT output (positive sequence direct trip)

e. OR36 output (two-out-of-three trip logic output)

f. Direct Transferred Trip (timer TL13 output)

The IR output, as its name implies, is only meant to inhibit reclosing, and is intended to be used in reclosing schemes where sequential reclosing is permitted.

Inputs "a" through "e" can be enabled/disabled through individual switches provided in the logic. Input "f" is present all of the time that a direct transferred trip signal is received.

Sequential Reclosing

In a sequential reclosing scheme, one end of the line is allowed to reclose first, and if that reclosure is successful then the other end of the line is allowed to follow. Hence, the name sequential reclosing. A prime reason for using sequential reclosing is to allow the end of the line at which the fault appears to be least severe to the system to close first so as to minimize the shock to the power system, if the reclosure proves unsuccessful.

The PLS system is well-suited to this type of application because the fault detectors used to activate the inhibit reclose circuit provide an indication of fault severity. For example, a positive sequence distance function will operate for all three-phase faults within its reach; and, depending on source impedance and reach setting, will also operate for some close-in, severe unbalanced faults[1]. The functions in the PLS system exhibit this type of performance but have the following features included:

PDT The PDT function, as described earlier, is provided with a zero sequence current restraint input that is used to prevent it from operating for close-in phase-to-ground faults. Thus, if the PDT input is used in the inhibit reclose circuit, it will inhibit reclosing for all three-phase faults on the line, and for some phase-to-phase and some phase-to-phase-to-ground faults. It will not inhibit for close-in SLG faults.

PDX The PDX function has a zero sequence current input that aids operation, rather than restrains it as in PDT, thus this function is more likely to operate for close-in severe SLG faults. It may be desirable to use this feature to inhibit reclosing at the ends of transmission lines located near a generating station, where, from a stability point of view, a close-in SLG fault may be as severe as any other type of fault further out on the line.

PD1 The PD1 function is set to reach short of the end of the transmission line when used as a pure distance function, or it is set to operate at certain level of operate signal when used in the combination overcurrent distance mode. Thus, this function will be limited in the number of three-phase faults that it sees on the line, and even more limited in the number of unbalanced faults that it sees. It will be an indication of a rather severe fault when it operates because of the limited setting that is used.

The ND input, and two-out-of-three logic input, can be used to energize the IR circuit to inhibit on the occurrence of even more unbalanced faults than can be detected by the positive sequence distance functions alone.

The 5 inputs (a through f) just described are sealed in by an output from any one of the undervoltage functions so that IR will stay energized as long as the undervoltage condition persists. For example, consider a phase-to-ground fault at F4 in Figure CS-10. Assume that the PDX functions at both ends of the line are set to inhibit reclosing, and further assume that only the PDX at line-end B operates. For this condition, line-end A will reclose in high speed. Line-end B cannot reclose until end A has reclosed successfully to allow the voltage to return to normal at end B to release the inhibit reclose output. When voltage returns to normal, indicating a successful reclosure, end B will be allowed to successfully reclose. Note that if there is no indication of fault severity at either end of the line, then each end will be allowed to reclose in high speed. On the other hand, if each end indicates that a severe fault has occurred, then sufficient time-delay should be added before reclosing is attempted, or reclosing should be blocked altogether.

The direct transferred trip (DTT) input to the IR circuit is not sealed in via an undervoltage output. This input comes from timer TL13 (security timer) in the logic and will last only as long as a transferred trip signal is received from the other end of the line. Thus, if the DTT input is initiated by the normal relaying at the other end of the line, the DTT signal will reset shortly after the fault is cleared at the other end. At that time, the IR circuit will be released unless a severe fault has been indicated as described above. If the DTT signal is initiated as a result of an equipment fault or breaker, the DTT signal will be received for a long time, or continually, and timer TL22 will time out to energize the lockout reclosing circuit to lockout reclosing.

Settings

The following settings must be made:

<u>BLOCK RI</u>	**ULM17-**
<u>INH REC-1, PDT</u>	**ULM18-**
<u>INH REC-2, PDX</u>	**ULM18-**
<u>INH REC-3, PD1</u>	**ULM18-**
<u>INH REC-4, ND</u>	**ULM18-**
<u>INH REC-4, 2/3</u>	**ULM18-**

CONTACT CONVERTERS

The following contact converters (CC-) are included in the system:

CC1 This contact converter is used for the permissive receiver input. See Figure CS-10 for external connections.

CC2 This contact converter is not used.

CC3 This contact converter is used for the direct transferred trip (DTT) channel input when tripping through the logic for a DTT is desired. If DTT tripping is not used, leave this CC unenergized.

CC5 This contact converter is used to arm the three-pole trip circuits when it is desired to initiate a three-pole trip regardless of fault type. It must be energized continuously when the scheme is applied for three-pole tripping only.

CC7 This contact converter is used to initiate a three-pole trip through the logic, but RI will not be blocked and the lockout reclose relay will not be energized. Use this CC if it is desired to trip through the logic and allow reclosing.

CC8 This contact converter is used to initiate a three-pole trip through the logic. The lockout reclose (LR) relay will be energized to block reclosing, and the reclose initiate (RI) relay will be blocked if the BLOCK RI switch is in the IN position. Use this CC if it is desired to trip through the PLS logic and block reclosing.

CC9 This contact converter is used to block all of the trip, BFI, RI and keying outputs. The green in service, "IN SERV" LED on the ULM17- module will also go out when CC9 is energized.

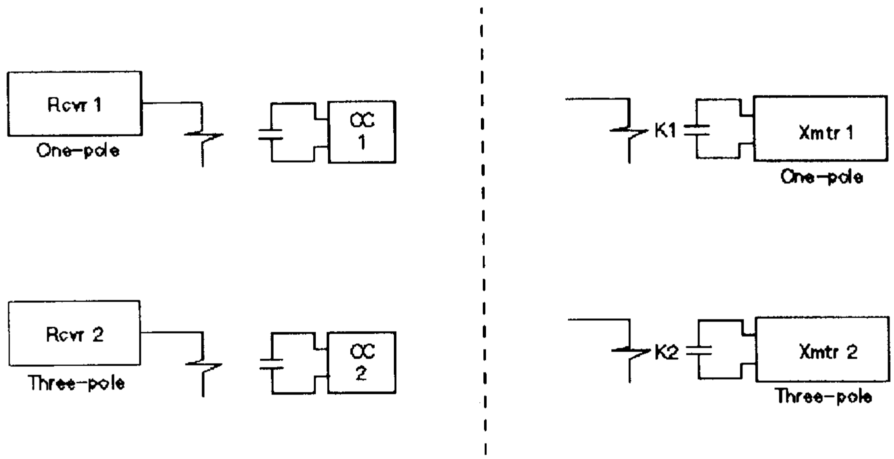
CC10 This contact converter is used to reset the red sealed in target lamps.

CC11 This contact converter is not used.

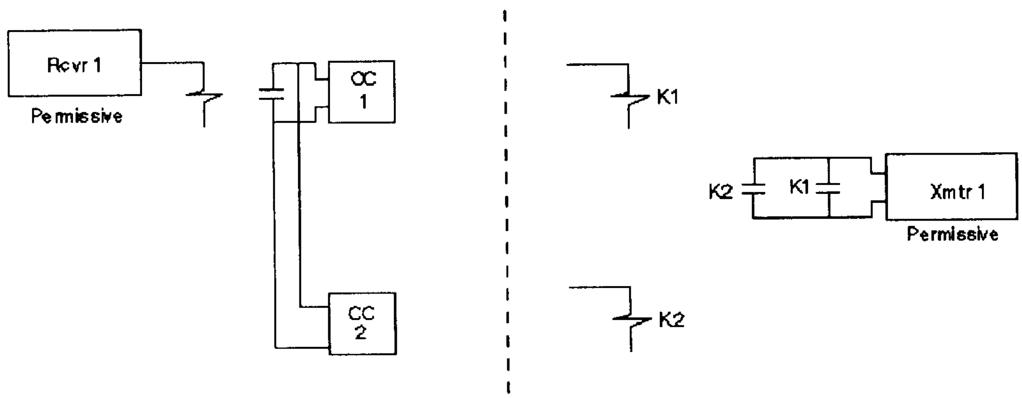
CC12 CC12 must be energized at both ends of the line in those applications where the ZS0/ZS1 ratio of the source impedance at either end of the transmission line is less than 0.75. This might occur, for example, on a line terminated at a large generating station. The output from CC12 does the following:

1. It permits any phase selector output to block three-pole trip selection by the PDT function.
2. It permits any phase selector output to block undervoltage phase selection during weak infeed conditions.

CC13 Leave this contact converter de-energized.



Connections When Two Communication Channels are Used



Connections When one Communication Channel is Used

Figure CS-10 Connections For Communications Channel(s)

CHANNEL KEYING OUTPUTS

The following outputs are provided. See Figure CS-10 for external connections.

Key Xmtr 1 (K1)

Two normally open contacts are provided for keying of the permissive transmitter.

Key Xmtr 2 (K2)

Two normally open contacts are provided for keying of the number 2 transmitter (for use in certain schemes). These contacts are not used in this scheme.

TABLE CS-2 PLS1B SETTINGS

Station:____________ Line:_______________

Module	Adjustment	Purpose	Location	Setting
ADM101	IB BIAS	IB pickup	on board	____
ADM101	IT BIAS	IT pickup	on board	____
ADM101	I0 SHUNT	IT adaptive restraint	on board	____
ADM101	KT	NT/NB compensation	on board	____
ADM101	I2 SHUNT	IT adaptive restraint	on board	____
AEM10-	IM	IMA,IMB,IMC pickup	on board	____
AEM10-	3I0	3I0 pickup	on board	____
AEM10-	PDX	PDX reach multiplier	on board	____
AEM111	I1	I1T pickup	on board	____
AEM111	VA2	NT/NB phase shift	on board	____
AEM111	ZR1	Replica impedance angle	on board	____
DNM10-	ND BIAS*	ND restraint bias	on board	____
DNM10-	N2	ND/NDD Z2 reach multiplier	on board	____
DNM10-	N3	ND/NDD Z3 reach multiplier	on board	____
DPM10-	ZT	PDT reach	on board	____
DPM10-	OFFSET	Forward offset	on board	____
DPM10-	PDB	PDB reach multiplier	on board	____
DPM10-	POSB	POSB reach multiplier	on board	____
DPM10-	PDB TC	PDB time constant	on board	____
DPM10-	PDT TC	PDT time constant	on board	____
DPM10-	POSB TC	POSB time constant	on board	____
DPM11-	Z1	PD1 reach	front pnl	____
DPM11-	DT PU	IDT pickup	on board	____
DPM11-	K0	IDT I0 compensation	on board	____
DPM11-	PD1 BIAS*	PD1 restraint bias	on board	____
DPM11-	TD	ITOC time dial	on board	____
DPM11-	TOC PU	ITOC pickup	on board	____
DPM11-	IDT DIR	IDT directional control	on board	____
DPM11-	IDT K1	IDT I1 restraint factor	on board	____
DPM11-	TOC DIR	ITOC directional control	on board	____
DPM11-	TOC K1	ITOC I1 restraint factor	on board	____
ULM15-	TL13	Direct transfer trip timer	on board	____
ULM15-	TL22	DTT reclose lockout timer	on board	____
ULM171	TL26	Coordination timer	on board	____
ULM171	BLOCK RI	RI control	on board	____
ULM181	INH REC	-1 PDT selection	on board	____
ULM181	INH REC	-2 PDX selection	on board	____
ULM181	INH REC	-3 PD1 selection	on board	____
ULM181	INH REC	-4 ND selection	on board	____
ULM181	INH REC	-5 3PT selection	on board	____

*Not used in Short Reach Schemes

PLS1B SETTINGS, continued

Station:____________ Line:______________

Module	Adjustment	Purpose	Location	Setting
ULM19-	ZONE 2	Zone 2 timer	front pnl	___
ULM19-	ZONE 3	Zone 3 timer	front pnl	___
ULM19-	WEAK INFEED	Weak infeed delay timer	front pnl	___
ULM19-	TL1	Integrator timer	on board	___
ULM19-	TL9	TL9 pickup time	on board	___
ULM19-	TL24	NB dropout time	on board	___
ULM19-	TL25	MB dropout time	on board	___
ULM19-	OSB-1	OSB block selection	on board	___
ULM19-	OSB-2	OSB block selection	on board	___

Hardware Description

HARDWARE DESCRIPTION

CASE ASSEMBLY

Construction

The case that houses the electronic modules is constructed from an aluminum alloy. It consists of a main frame with side mounting brackets, a front cover and a rear cover.

The front cover, comprised of a metal frame with plate glass, is pivoted on the top and is opened from the bottom by way of two spring-loaded latches. The door is constrained from coming off by tabs that require the door to be unlatched and lifted slightly in order to be removed.

The rear cover supports terminal blocks that are used in making external connections to the case.

The modules are mounted vertically inside the case and they are supported by sockets within the case. In addition to this mechanical support, the sockets also offer the means of making the electrical connection to the modules. The modules are further restrained inside the case by the front cover.

Proper alignment of the module with respect to the socket is maintained by slotted guides, one guide above and one guide beneath each module, with the exception of the magnetics module, MGM, which requires two guides above and two beneath.

Electrical Connections and Internal Wiring

External connections are made to each case through twelve terminal blocks mounted on the rear cover plate. Each block contains 14 terminal points, which consist of a Number 6 screw threaded into a flat contact plate.

Connection to the printed circuit board modules is made by means of 60-pin edge connectors. Connection to the MGM module is made by means of two connector sockets; an 8-contact current block and a 104-pin signal block. The current block contacts are rated to handle current transformer (CT) secondary currents, and they are shorted upon removal of the MGM module.

Identification

The PLS system model number label is located on the inside of the front cover.

A marking strip indicating the name and position of every module in a case is included on the lower bar. It is placed to be read when the front cover is removed. Figure MO-1 shows the location of the modules.

The terminal blocks located on the rear of the modular case are uniquely identified by a two letter code that is found directly beneath the outer-most edge of each terminal block. Also, the terminal points (1 through 14) are identified by stamped numbers.

PRINTED CIRCUIT BOARD MODULES

Basic Construction

Each module consists of a printed circuit board and front panel. Two knobs are provided on the front panel for removing and inserting the module. Electrical connection is made by the contact pads at the back edge of the board. Not all module locations within the case have a printed circuit board. Some locations have a blank board and front panel.

Identification

Each module has its own identification number consisting of a three letter code followed by a three digit number. These are found at the bottom of each front panel and may be read when the case cover is removed.

RECEIVING, HANDLING AND STORAGE

CAUTION

This relay contains electronic components which could be damaged by electrostatic discharge currents if those currents flow through certain terminals of the components. The main source of electrostatic discharge currents is the human body, and the conditions of low humidity, carpeted floors and isolating shoes are conducive to the generation of electrostatic discharge currents. Where these conditions exist, care should be exercised when removing and handling the modules to make settings on the internal switches. The persons handling the module should make sure that their body charge has been discharged by touching some surface at ground potential before touching any of the components on the modules.

Immediately upon receipt, the equipment should be unpacked and examined for any damage sustained in transit. If damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

If the equipment is not to be installed immediately, it should be stored indoors in a location that is dry and protected from dust, metallic chips, and severe atmospheric conditions.

INSTALLATION

Environment

The location should be clean and dry, free from dust and excessive vibration, and well lighted to facilitate inspection and testing.

Mounting

The PLS case has been designed for standard rack mounting. The case measures eight rack units in height. Refer to Figure HD-3 for the outline and mounting dimensions.

External Connections

External connections are made according to the elementary diagram, Figure SD-4. This is a general diagram incorporating all of the available options. Connection need not be made to those terminals associated with options that will not be used. External and temporary jumper connections for acceptance and periodic testing are located at the end of the Acceptance Test section. When Test Point pins 55 and 60 are jumpered with an external jumper, the FD LED will illuminate, and the Red Continuous Monitor LED will flash throughout testing of the relay.

SURGE GROUND CONNECTIONS

WARNING

PLS TERMINALS BH13 AND BH14 MUST BE TIED TOGETHER, AND TERMINAL BH14 MUST BE TIED TO THE GROUND, BUS AS SHOWN IN THE ELEMENTARY DIAGRAM, FIGURE SD-4. THE CONNECTION TO THE GROUND BUS MUST BE MADE USING A NO. 12 WIRE OR LARGER. THE LEADS USED IN MAKING BOTH OF THESE CONNECTIONS SHOULD BE AS SHORT AS POSSIBLE.

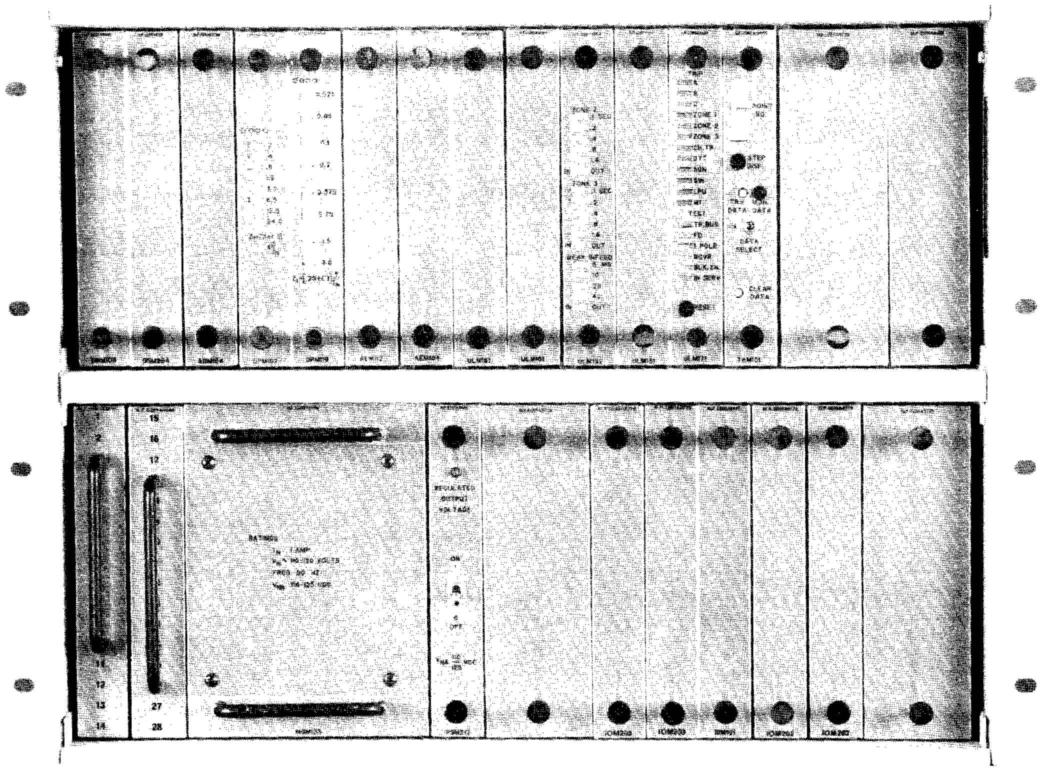


Figure HD-1 (8043804) PLS Relaying System, Front View

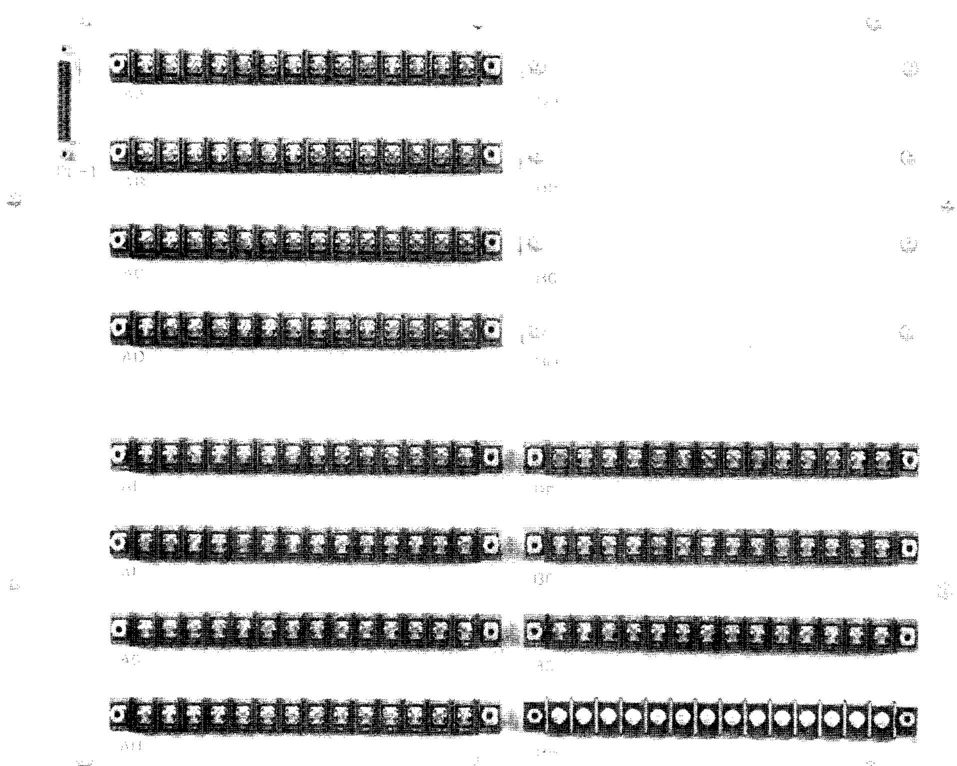


Figure HD-2 (8043803) PLS Relaying System, Rear View

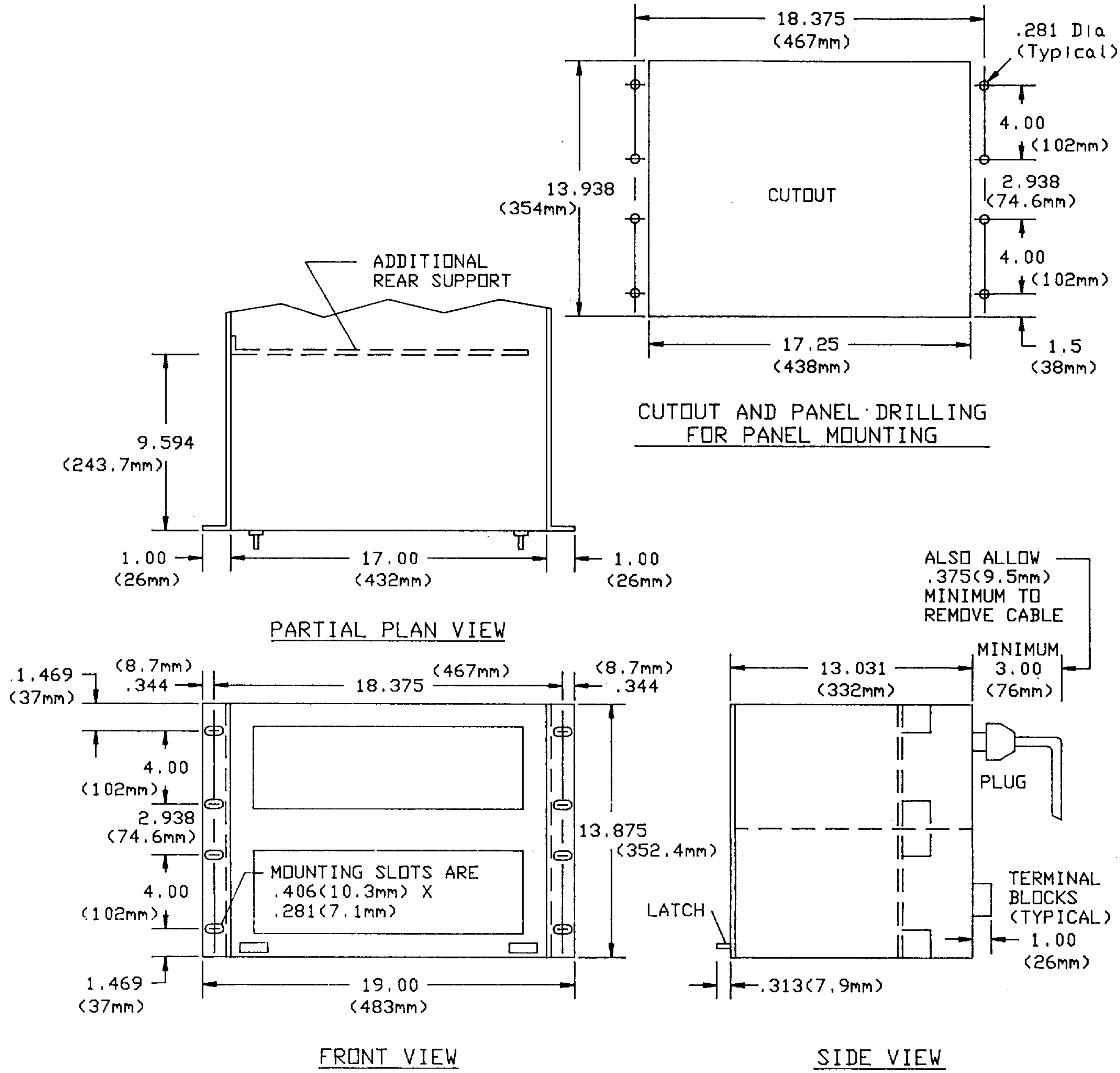
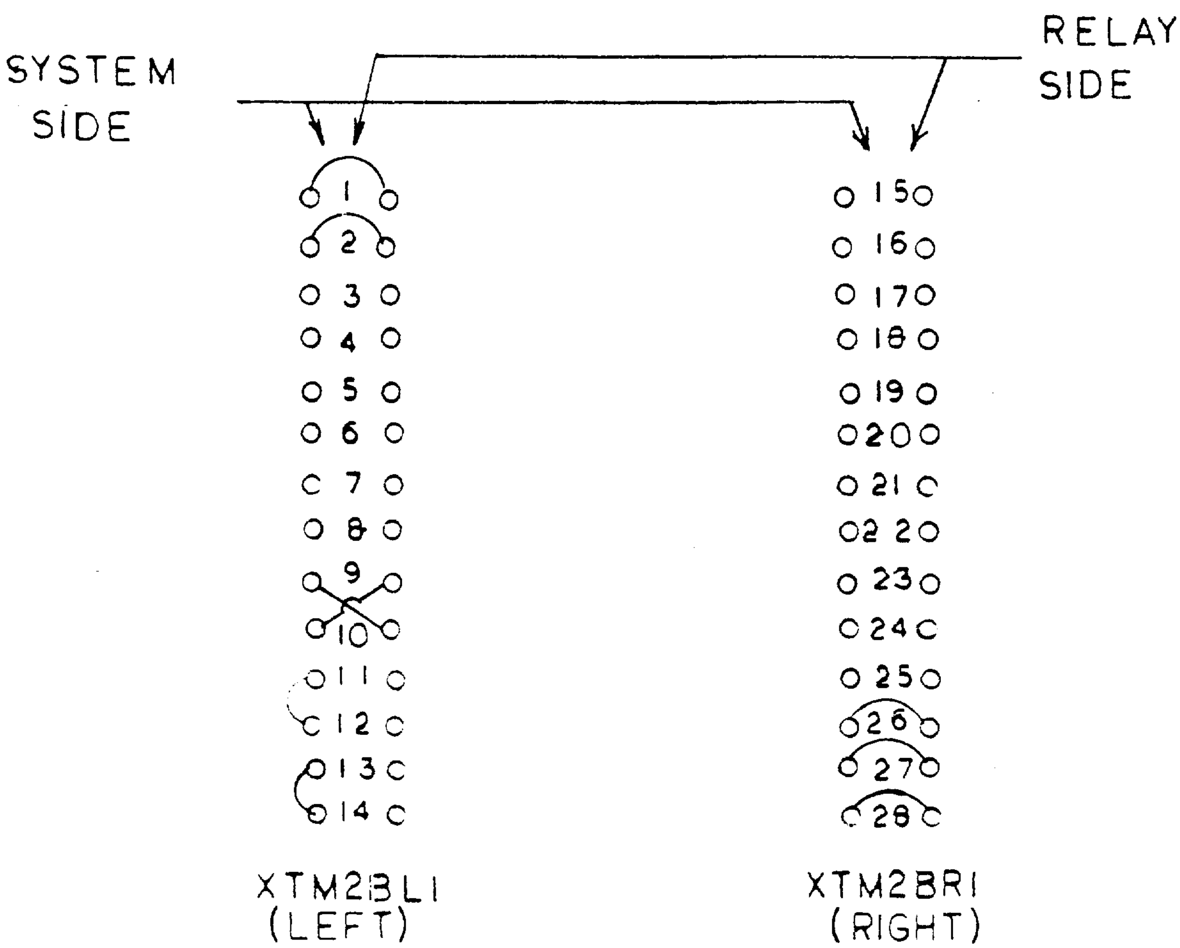


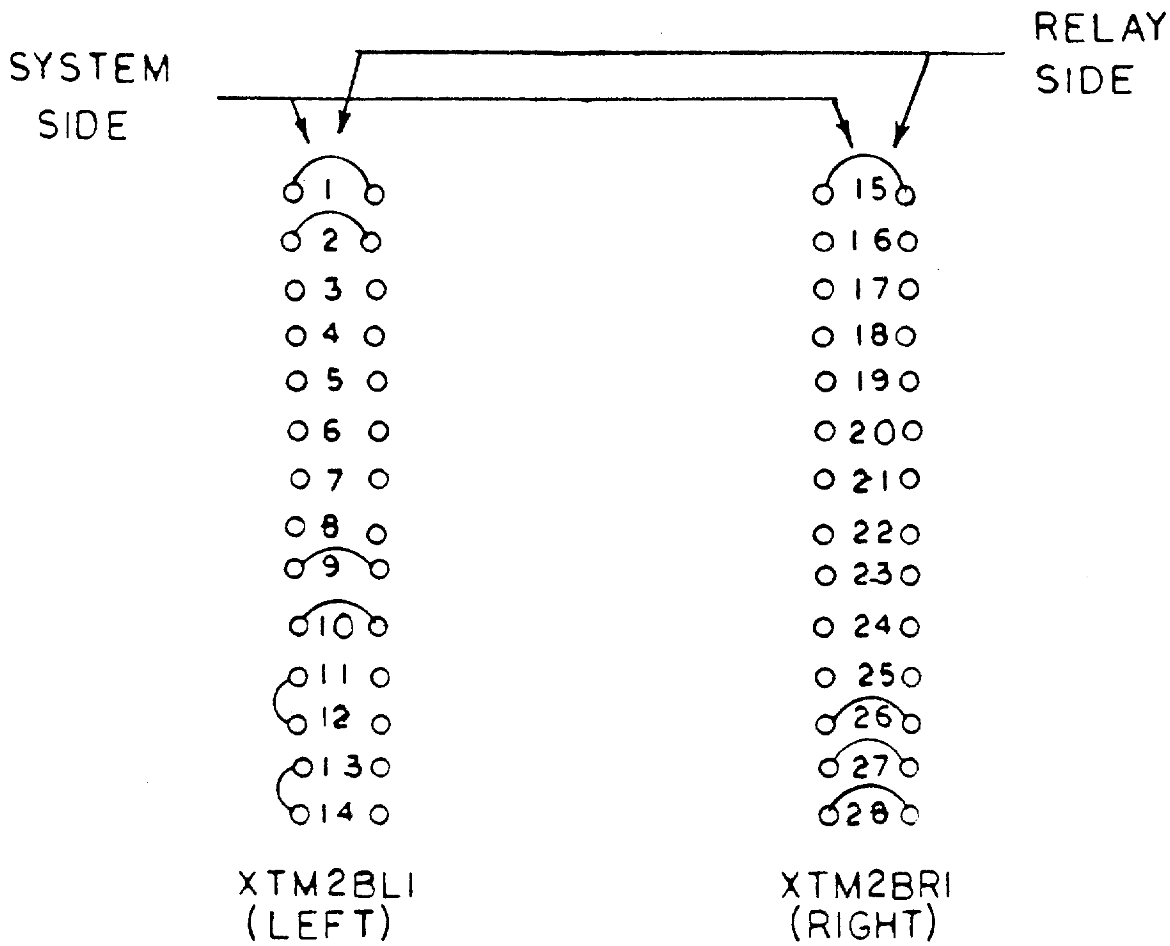
Figure HD-3 (0184B6393 [1]) Outline and Mounting Dimensions



CAUTION:

CONNECTIONS BETWEEN POINTS 9 THROUGH 14 MUST BE MADE BEFORE INSERTING THE XTM TEST PLUG TO PREVENT OPEN CIRCUITING THE CT SECONDARIES.

Figure HD-4 (0285A9895) XTM Connections for Directional Check (Tripping Direction)



CAUTION:

CONNECTIONS BETWEEN POINTS 9 THROUGH 14 MUST BE MADE BEFORE INSERTING THE XTM TEST PLUG TO PREVENT OPEN CIRCUITING THE CT SECONDARIES.

Figure HD-5 (0285A9896) XTM Connections for Directional Check (Non-Trip Direction)

Modules

MODULE DESCRIPTION

Refer to the **CALCULATION OF SETTINGS** section for determination of module settings.

ADM10- (See Figure MO-2)

This module provides the following functions:

1. Directional unit for directional overcurrent channel tripping (NT)
2. Overcurrent unit for directional overcurrent channel tripping (IT)
3. Directional unit for directional overcurrent channel blocking (NB)
4. Overcurrent unit for directional overcurrent channel blocking (IB)

On-Board Switches

IB BIAS	These switches adjust the pickup level of the IB unit. The operating signal is $(2|I_0| + |I_2|-0.2|I_1|)$ where $|I_0|$ indicates the magnitude of zero- sequence current. Pickup is in per unit of I_N and is adjustable from 0.05 to 0.755 per unit in steps of 0.025 per unit. The per unit pickup current is equal to 0.05 plus the sum of the closed (toggle to the right) switches.
IT BIAS	These switches adjust the pickup level of the IT unit. The operating signal is $(2|I_0| + |I_2|-0.3|I1|)$ where $|I_0|$ indicates the magnitude of zero-sequence current. Pickup is in per unit of I_N, and is adjustable from 0.05 to 0.755 per unit in steps of 0.025 per unit. The per unit pickup current is equal to 0.05 plus the sum of the closed (toggle to the right) switches.
I0 SHUNT	These switches compensate the pickup level of the IT unit for the zero-sequence current in the shunt capacitance of the transmission line. The compensation is in per unit of rated current (I_N) and is adjustable from 0.01 to 0.63 per unit in steps of 0.02 per unit. The per unit compensation is equal to 0.01 plus the sum of the closed (toggle to the right) switches.
I_2 SHUNT	These switches compensate the pickup level of the IB and IT units for the negative-sequence current in the shunt capacitance of the transmission line. The compensation is in per unit of rated current (I_N) and is adjustable from 0.01 to 0.63 per unit in steps of 0.02 per unit. The per unit compensation is equal to 0.01 plus the sum of the closed (toggle to the right) switches.
KT	These switches adjust the current compensation for the NT and NB units. Compensation is in per unit of reach and is adjustable from 0 to 1 per unit in steps of 0.05 per unit. The per unit compensation is equal to 0 plus the sum of the closed (toggle to the right) switches.

AEM10- (See Figure MO-3)

These modules provide the following functions:

1. Zone 2 positive-sequence distance unit (PDX)
2. Phase current level detectors (IMA, IMB, IMC)
3. Zero-sequence current level detector (3I0)
4. Phase undervoltage detectors (VA, VB, VC)

On-Board Switches

IM These switches adjust the pickup level of the IMA, IMB and IMC level detectors. Pickup is in per unit of rated current (I_N) and is adjustable from 0.1 to 1.0 per unit in steps of 0.05 per unit. The per unit pickup is equal to 0.1 plus the sum of the closed (toggle to the right) switches.

3I0 These switches adjust the pickup level of the $3I_0$ level detector. Pickup is in per unit of rated current (I_N) and is adjustable from 0.1 to 0.7 per unit in steps of 0.2 per unit. The per unit pickup is equal to 0.1 plus the sum of the closed (toggle to the right) switches.

PDX These switches select the reach of the PDX unit in multiples of the Zone 1 reach (which is set on the front panel of the DPM11- module). This reach multiplier is adjustable from 1 to 2.5 in steps of 0.1, and is equal to 1 plus the sum of the closed (toggle to the right) switches.

AEM11- (See Figure MO-4)

These modules provide the following functions.

1. Fault detector (FD)

2. Positive-sequence current level detector (I1T)

On-Board Switches

I1 These switches adjust the pickup level of the I1T level detector. Pickup is in per unit of rated current (I_N) and is adjustable from 0.2 to 3.2 per unit in steps of 0.2 per unit. The per unit pickup is equal to 0.2 plus the sum of the closed (toggle to the right) switches.

VA2 These switches provide an adjustable leading phase shift in the negative- sequence voltage signal for the NT and NB units. This phase shift is adjustable from 0° to 30° in 10° Steps. The phase shift is equal to 0 plus the sum of the closed (toggle to the right) switches.

ZR1 These switches select the replica impedance angle for the distance measuring units. The replica impedance angle can be selected from 70° to 85° in 5° steps. The characteristic angle is equal to 70 plus the sum the of closed (toggle to the right) switches.

DNM10- (See Figure MO-5)

These modules provide the ND and NDD functions.

On-Board Switches

ND BIAS These switches provide an adjustable restraint bias to prevent overreach of the ND unit due to series capacitors. The bias is in per unit with a base voltage of 67 volts RMS line-to-neutral, and is adjustable from 0 to 1.6 per unit in steps of 0.03 per unit. The per unit bias is equal to 0 plus the sum of the closed (toggle to the right) switches.

N2 These switches select the zone 2 reach of the ND and NDD units in multiples of the zone 1 reach (which is set on the front panel of the DPM11- module). This reach multiplier is adjustable from 1 to 2.5 in steps of 0.1 and is equal to 1 plus the sum of the closed (toggle to the right) switches.

N3 These switches select the zone 3 reach of the ND and NDD units in multiples of the zone 1 reach (which is set on the front panel of the DPM11- module). This reach multiplier is adjustable from 1 to 4.75 in steps of 0.25, and is equal to 1 plus the sum of the closed (toggle to the right) switches.

DPM10- (See Figure MO-6)

These modules provide the following functions:

1. Overreaching positive-sequence distance unit (PDT)
2. Blocking positive-sequence distance unit (PDB)
3. Out-of-step blocking unit (POSB)

Front Panel Switches

ZT These switches adjust the positive-sequence reach of the PDT unit directly, and they also affect the reach of the PDB and POSB units. The reach of 5-ampere- rated relays is adjustable from 2 to 50 ohms in 0.2 ohm steps. The reach is equal to 2 plus the sum of the closed (toggle to the right) switches .

For relays rated 1 ampere, the reach will be 5 times the value determined by the above method.

On-Board Switches

OFFSET These switches select the per unit offset (into the protected line section) of the polarizing voltage for the positive-sequence distance units. The offset is adjustable from 0 to 0.3 per unit in 0.1 per unit steps and is equal to 0 plus the sum of the closed (toggle to the right) switches.

PDB These switches select the positive-sequence reach of the PDB unit in multiples of the PDT reach (which is set on the front panel of this module). This reach multiplier is adjustable from 0.5 to 2.25 in steps of 0.25 and is equal to 0.5 plus the sum of the closed (toggle to the right) switches.

POSB These switches select the positive-sequence reach of the POSB unit in multiples of the PDT reach (which is set on the front panel of this module). This reach multiplier is adjustable from 1 to 2.5 in steps of 0.1 and is equal to 1 plus the sum of the closed (toggle to the right) switches.

On-Board Links

PDB TC This link selects the time constant for the integrator of the PDB unit. A SHORT and a LONG position are provided.

PDT TC This link selects the time constant for the integrator of the PDT unit. A SHORT and a LONG position are provided.

POSB TC This link selects the time constant for the integrator of the POSB unit. A SHORT and a LONG position are provided.

DPM11- (See Figure MO-7)

These modules provide the following functions:

1. Zone 1 positive-sequence distance unit (PD1)
2. Direct trip overcurrent unit (IDT)
3. Time overcurrent unit (TOC)

Front Panel Switches

Z1 These switches adjust the positive-sequence reach of the PD1, ND and NDD units, and they also affect the reach of the PDX unit. The reach of 5-ampere-rated relays is adjustable from 1 to 25 ohms in 0.1 ohm steps, and is equal to 1 plus the sum of the closed (toggle to the right) switches.

For relays rated 1 ampere, the reach will be 5 times the value determined by the above method.

On-Board Switches

DT PU These switches adjust the pickup level of the IDT unit. The operating signal is $(3|I_0|-K1|I1|)$ where $|I_0|$ indicates the magnitude of the zero- sequence current and K1 is a constant equal to either 0 or 1, as selected by the "IDT K1" link. Pickup is in per unit of I_N and is adjustable from 0.4 to 4.0 per unit in 0.1 per unit. The per unit pickup current is equal to 0.4 plus the sum of the closed (toggle to the right) switches.

K0 These switches select the zero-sequence current compensation for the IDT unit. Compensation is adjustable from 1 to 7 per unit in steps of 0.1 per unit and is equal to 1 plus the sum of the closed (toggle to the right) switches.

PD1 BIAS These switches provide an adjustable restraint bias to prevent transient overreach of the PD1 unit due to series capacitors. The bias is in per unit with a base voltage of 67 volts RMS line-to-neutral and is adjustable from 0 to 1.6 per unit in steps of 0.03 per unit. The per unit bias is equal to 0 plus the sum of the closed (toggle to the right) switches.

TD These switches select the time-dial setting for the TOC unit. Time delay, at a given multiple of pickup current, increases directly as the time-dial setting increases. The time dial is adjustable from 0.5 to 10 in 0.5 and is equal to 0.5 plus the sum of the closed (toggle to the right) switches.

TOC PU These switches adjust the pickup level of the TOC unit. The operating signal is $(3|I_0|-K1|I_1|)$ where $|I_0|$ indicates the magnitude of the zero-sequence current and K1 is a constant equal either to 0 or 0.45, as selected by the "TOC K1" link. Pickup is in per unit of I_N and is adjustable from 0.05 to 0.6 per unit in 0.05 steps. The per unit pickup current is equal to 0.05 plus the sum of the closed (toggle to the right) switches.

On-Board Links

IDT DIR This link selects whether the IDT unit has directional control (DIR position) or does not have directional control (NON-DIR position). It also has an OFF position that disables the IDT unit completely.

IDT K1 This link selects "K1" for the IDT unit, which can be either 0 or 1.

TOC DIR This link selects whether the TOC unit has directional control (DIR position) or does not have directional control (NON-DIR position).

TOC K1 This link selects "K1" for the TOC unit, which can be either 0 or 0.45.

DSM20-

These modules provide the phase selection function.

There are no adjustments on these modules.

TAM101 (See Figure MO-8)

Refer to Continuous Monitor (CM) Section for a detailed description of how to use the Continuous Monitor Module.

ULM15- (See Figure MO-9)

The ULM15- module contains the channel keying, receiver, and phase selection logic. The combinational logic is implemented with programmable logic devices (PLD) which are socket-mounted. The transfer trip timers, TL13 and TL22, are also located on this board.

On-Board Adjustments

TL13 Transfer trip coordination delay time.

Range: 0 to 15 milliseconds in 1 millisecond steps. The operating time is the sum of the closed (toggle to the right) switches.

TL22 Delay to reclose lockout from the receipt of a transfer trip.

Range: 0 to 3.1 seconds in 0.1 second steps. The operating time is the sum of the closed (toggle to the right) switches.

ULM161

The ULM161 module provides the supervision logic for the measuring units. There are no adjustments on this board.

ULM171 (See Figure MO-10)

The ULM171 provides the targeting and output buffering for the scheme. There are two classes of targets, sealed-in (red) and monitor (amber). The red, or sealed- in, targets only light while the trip bus is energized, and retain the trip information for the last trip as long as the unit remains powered. The targets reset automatically on power up, or if a local or remote reset signal is given. The monitor targets are provided to simplify testing and indicate the status of the indicated point.

A local reset also initiates a lamp test; all indicators on this module will remain lit while the reset button is depressed. See Table MO-1 for a description of each target.

On-Board Adjustments

TL26 Supervision timer

Range: 0 to 77.5 milliseconds in 2.5 millisecond steps. The operating time is the sum of the closed (toggle to the right) switches.

Block RI

This switch chooses whether or not reclose initiation is blocked by lockout reclose. With the toggle to the left, reclose initiation is NOT blocked by lockout reclose; when the toggle is to the right, reclose initiation IS blocked by reclose lockout.

TABLE M0-1

Panel Marking	Color	Description
A	Red	Phase A fault
B	Red	Phase B fault
C	Red	Phase C fault
ZONE 1	Red	Trip via PD1, ND, IDT or ITOC
ZONE 2	Red	Trip via Zone 2 timer
ZONE 3	Red	Trip via Zone 3 timer
CH. TR.	Red	Channel trip or channel received during Zone 1 trip
DTT	Red	Transfer trip via TL13
50N	Red	Overcurrent direct trip (IDT)
51N	Red	Time overcurrent trip (ITOC)
LPU	Red	Line pickup trip
WI	Red	Weak infeed trip via TL16
TR. BUS	Amber	Trip bus operated
FD	Amber	Fault detector operated
3 POLE	Amber	3-pole trip selected
RCVR	Amber	Channel received
BLK ZN.	Amber	Blocking zone operated
IN SERV	Green	Unit in operable state

ULM181 (See Figure MO-11)

The ULM181 module contains the three-pole, inhibit reclose and lockout reclose logic and the line-pickup timers and logic.

On-Board Adjustment

INHIBIT RECLOSE

Choose what units will inhibit reclosing:

Switch position 1	PDT unit
Switch position 2	PDX unit
Switch position 3	PD1 unit
Switch position 4	ND unit
Switch position 5	3-pole trip

ULM19- (See Figure MO-12)

The ULM19- module provides the logic for First, Second, Third and Blocking Zone, Channel, Weak Infeed and Out-of-step Block.

Front Panel Adjustments

ZONE 2 Zone 2 (TL2) timer setting

Range: 0 to 3.1 seconds in 0.1 second steps. The operating time is the sum of the closed (toggle to the right) switches. The last switch is labeled IN/OUT. The timer is in service when this switch is set to IN, and out of service when it is set to OUT.

ZONE 3 Zone 3 (TL3) timer setting

Range: 0 to 3.1 seconds in 0.1 second steps. The operating time is the sum of the closed (toggle to the right) switches. The last switch is labeled IN/OUT. The timer is in service when this switch is set to IN, and out of service when it is set to OUT.

WEAK INFEED Weak infeed (TL16) timer setting

Range: 0 to 75 milliseconds in 5 millisecond steps. The operating time is the sum of the closed (toggle to the right) switches. The last switch is labeled IN/OUT. The timer is in service when this switch is set to IN, and out of service when it is set to OUT.

On-Board Settings

TL1 Trip integrator timer setting

Range: 0 to 15.5 milliseconds in 0.5 millisecond steps. The operating time is the sum of the closed (toggle to the right) switches.

TL9 Time delay to blocking of repeat keying from operation of the blocking unit

Range: 0 to 15 milliseconds in 1 millisecond steps. The operating time is the sum of the closed (toggle to the right) switches.

TL24 NB/IB blocking unit dropout time setting

Range: 10 to 120 milliseconds in 10 millisecond steps. The reset time is 10 plus the sum of the closed (toggle to the right) switches.

TL25 PDB blocking unit dropout time setting

Range: 40 to 210 milliseconds. The reset time is 39 plus the sum of the closed (toggle to the right) switches.

OSB Select functions blocked by the out-of-step unit

OSB-2 Blocks all tripping and OSB-1 functions when set to the right
OSB-1 Blocks all transmitter keying, PD1, and pilot tripping, and zone 2 and zone 3 timers.

PSM21- (See Figure MO-13)

The PSM21- module converts station battery to a usable DC voltage.

Front Panel Adjustments

ON-OFF toggle switch with a green LED that illuminates when the power supply is operating

A 3AG fuse is located on the module and is accessible for user replacement if necessary.

Power Supply Outputs:

12V, 1A
24V, 1A
NO, NC Power Supply Alarm Contacts

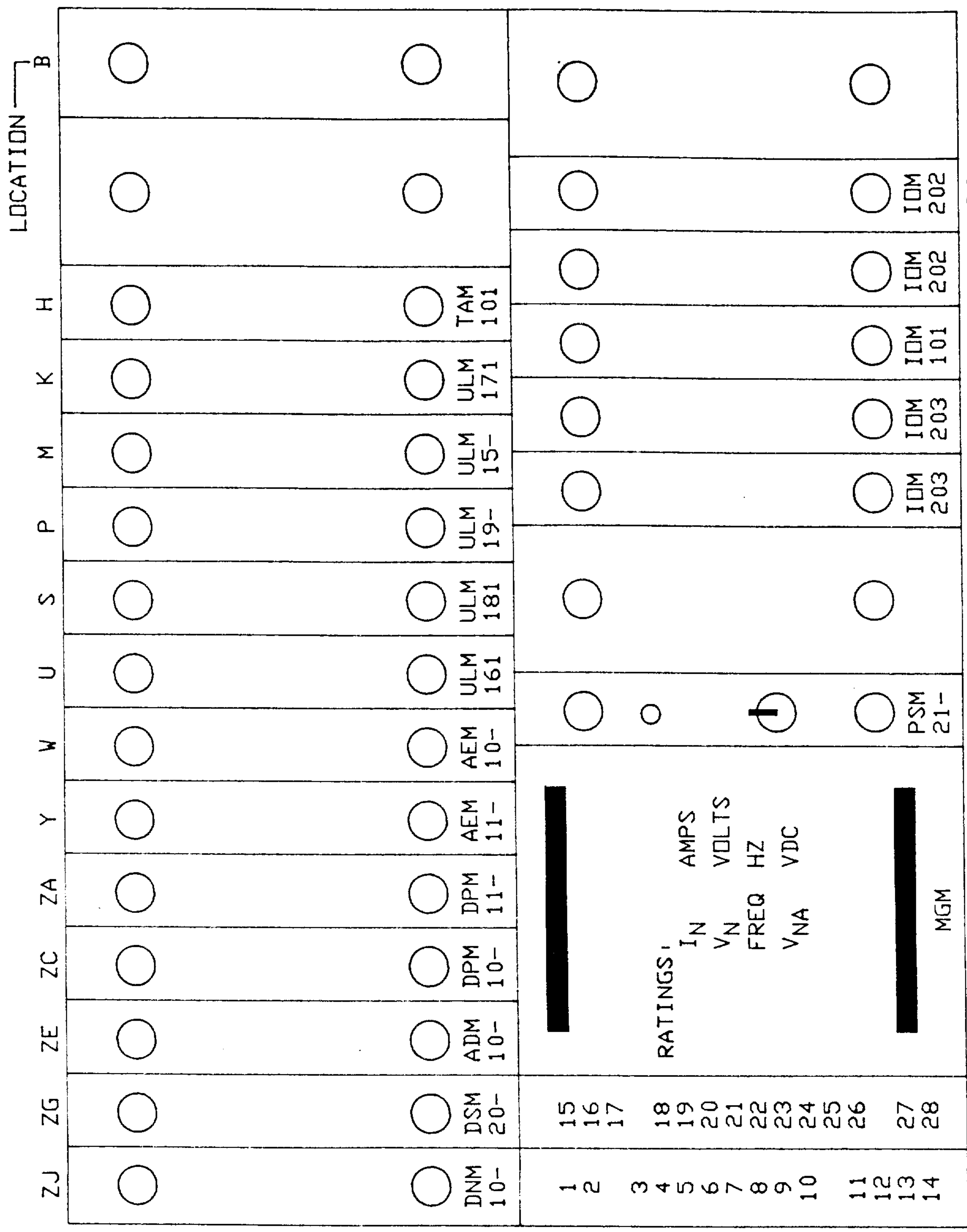


Figure MO-1 (0285A9823 [1]) Module Locations

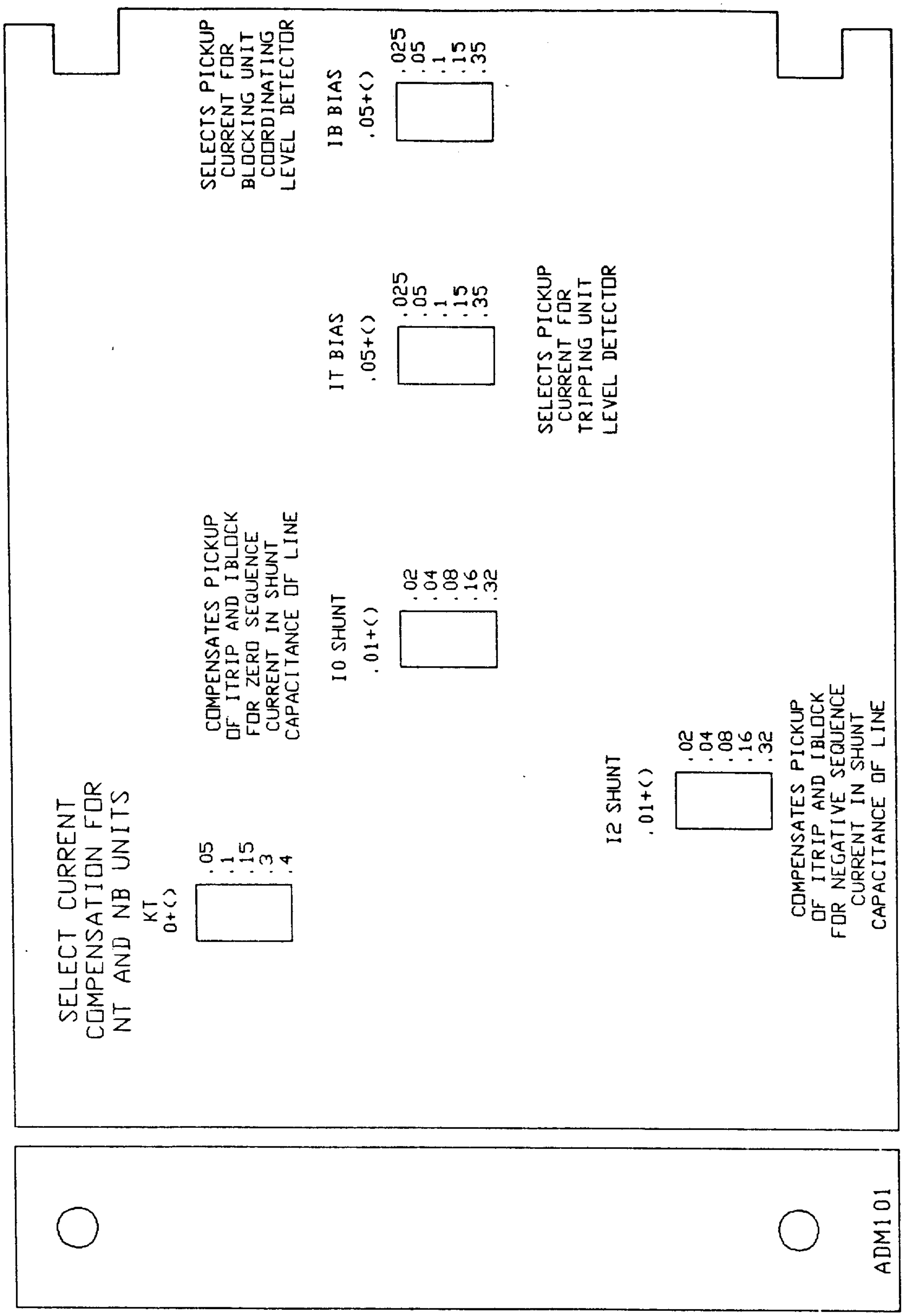


Figure MO-2 (0285A9825 [2]) ADM10-

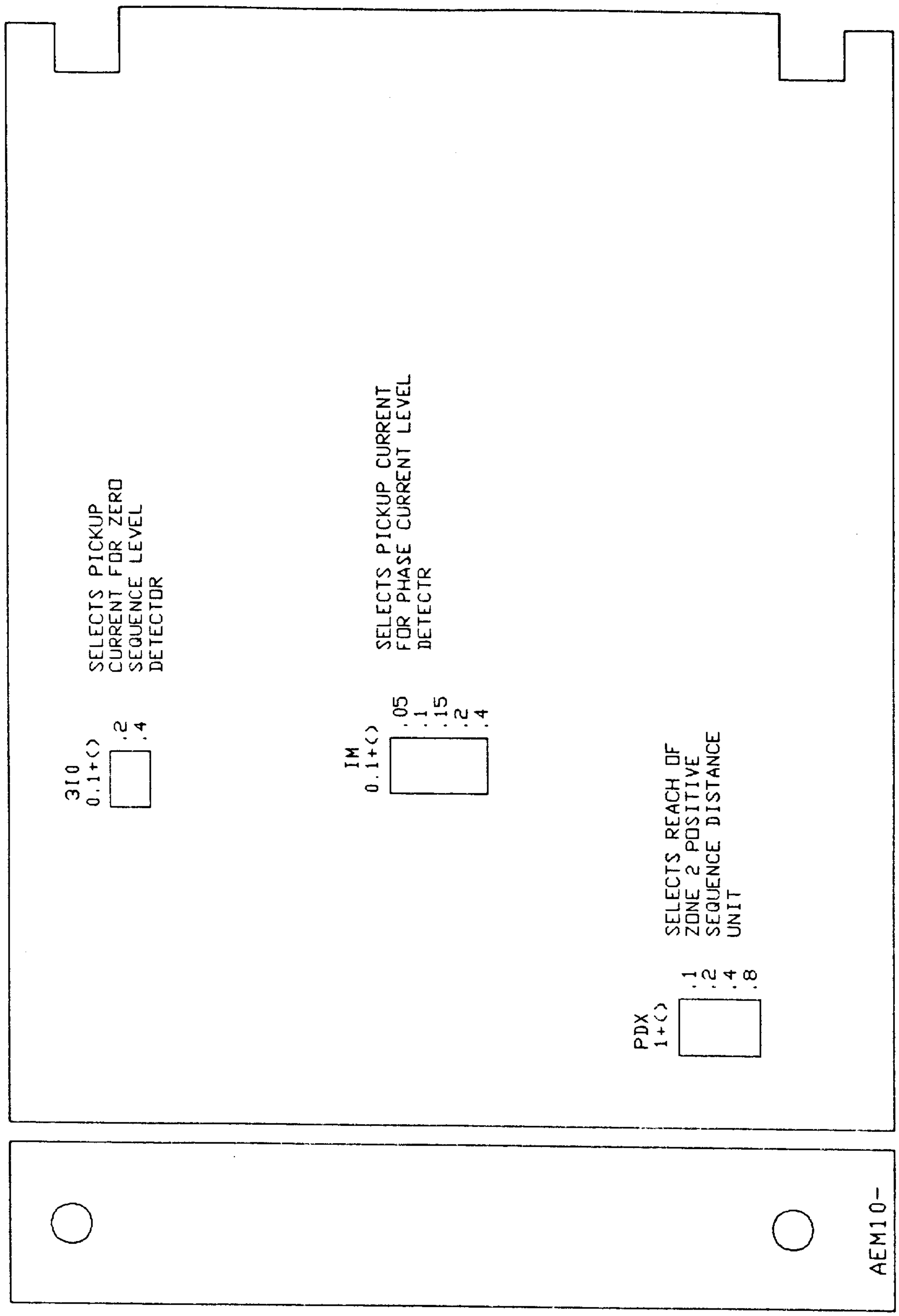


Figure MO-3 (0285A9826 [2]) AEM10-

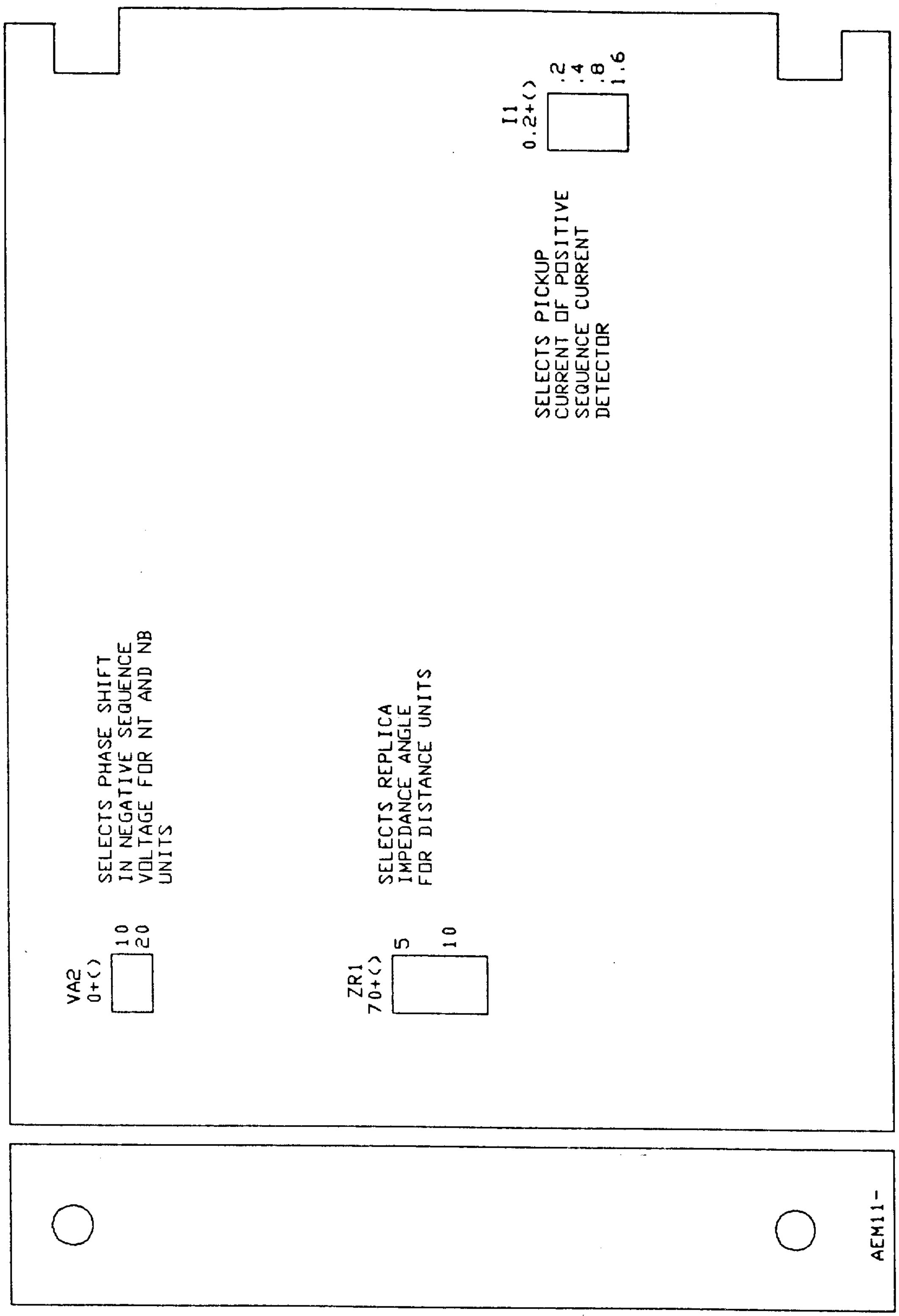


Figure MO-4 (0285A9827 [1]) AEM11-

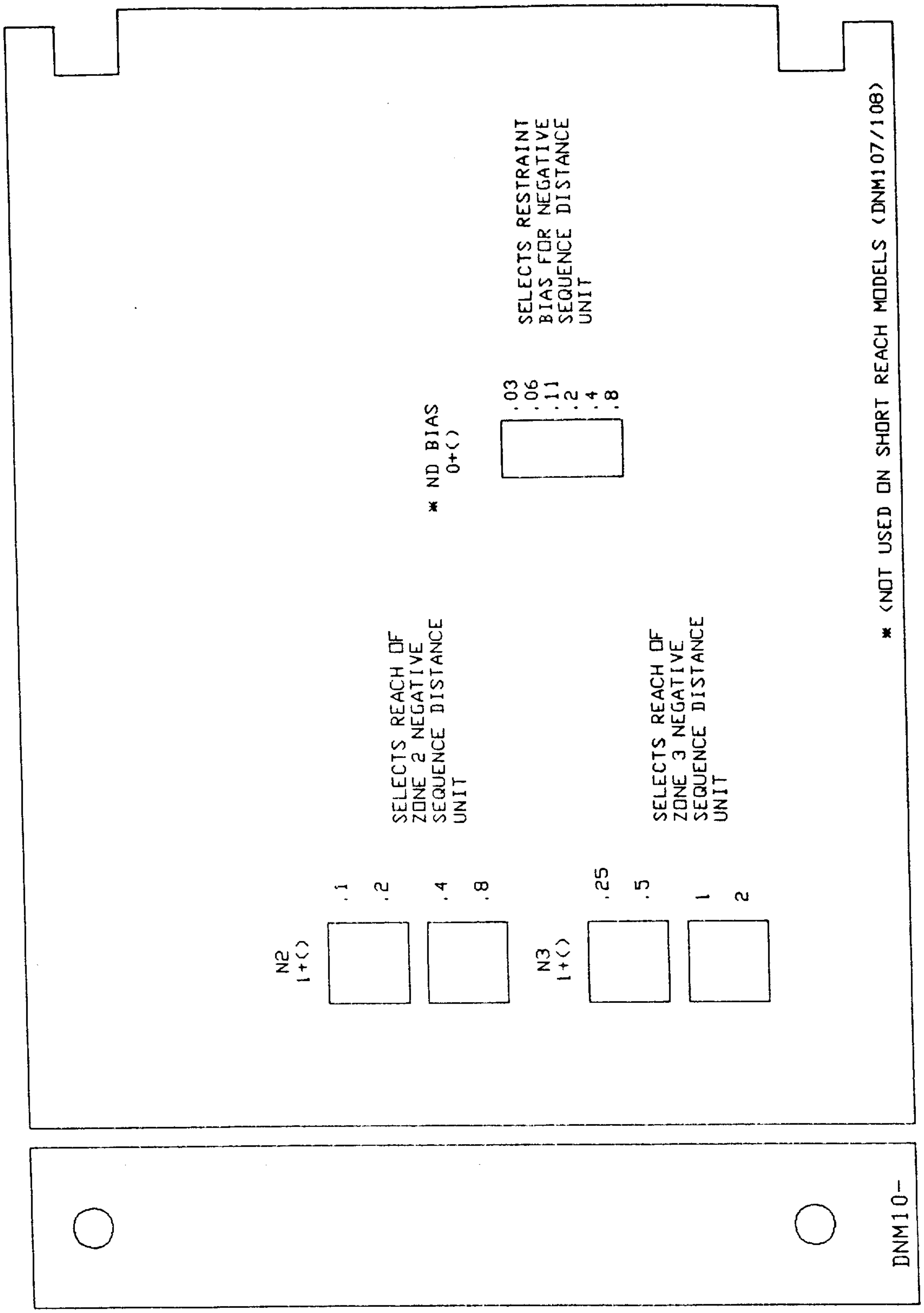


Figure MO-5 (0285A9828 [1]) DNM10-

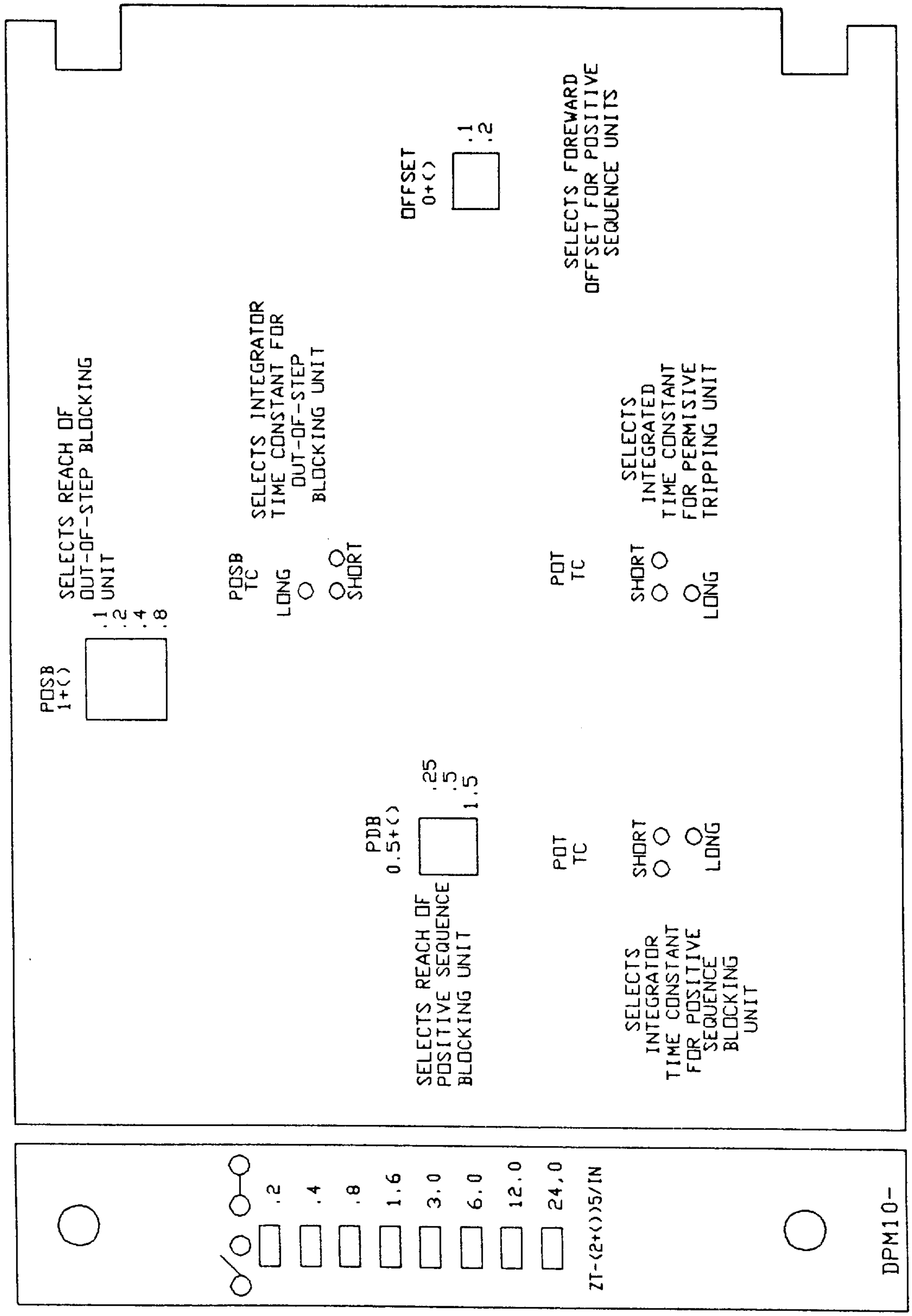


Figure MO-6 (0285A9829 [1]) DPM10-

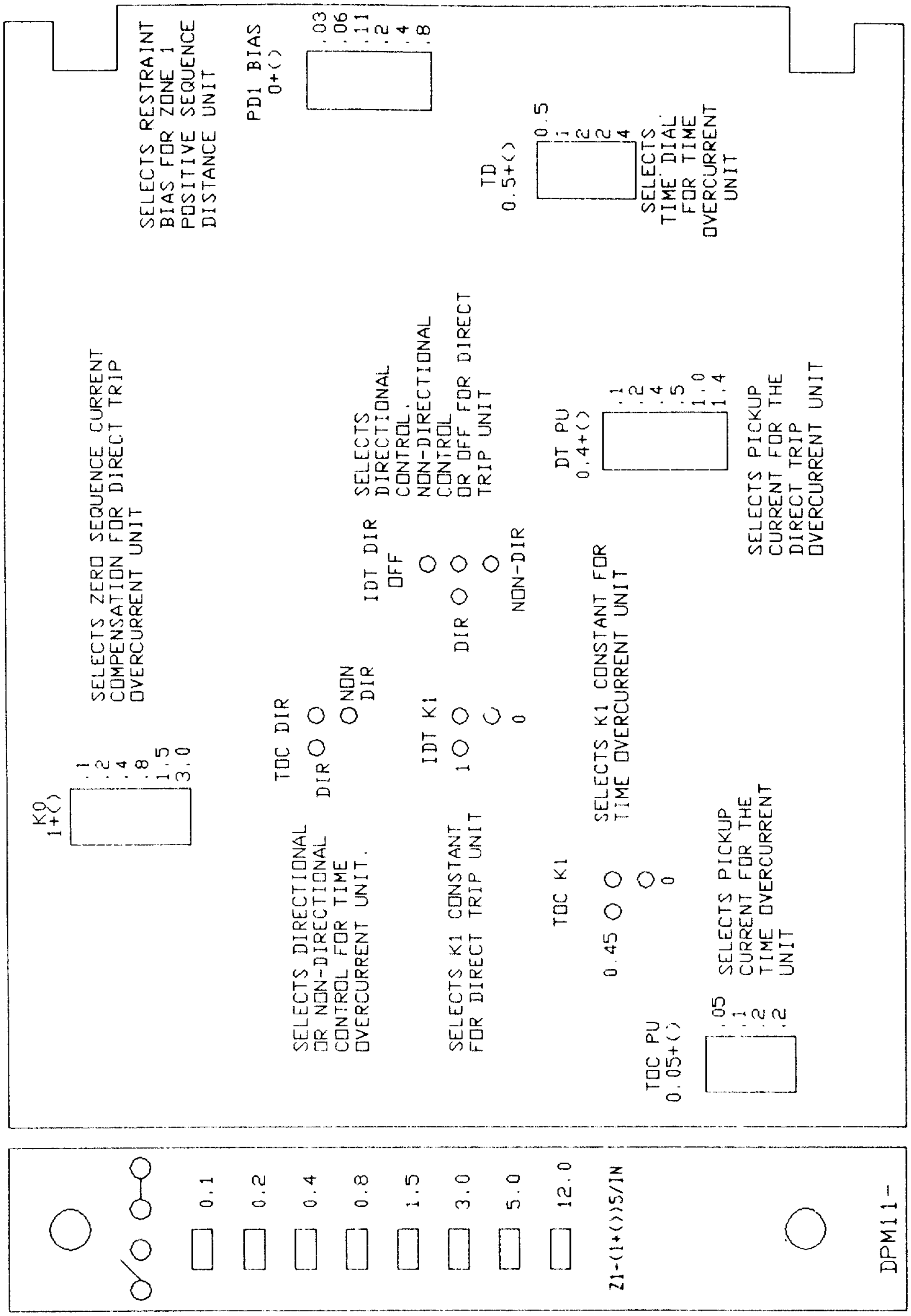


Figure MO-7 (0285A9830 [1]) DPM11-

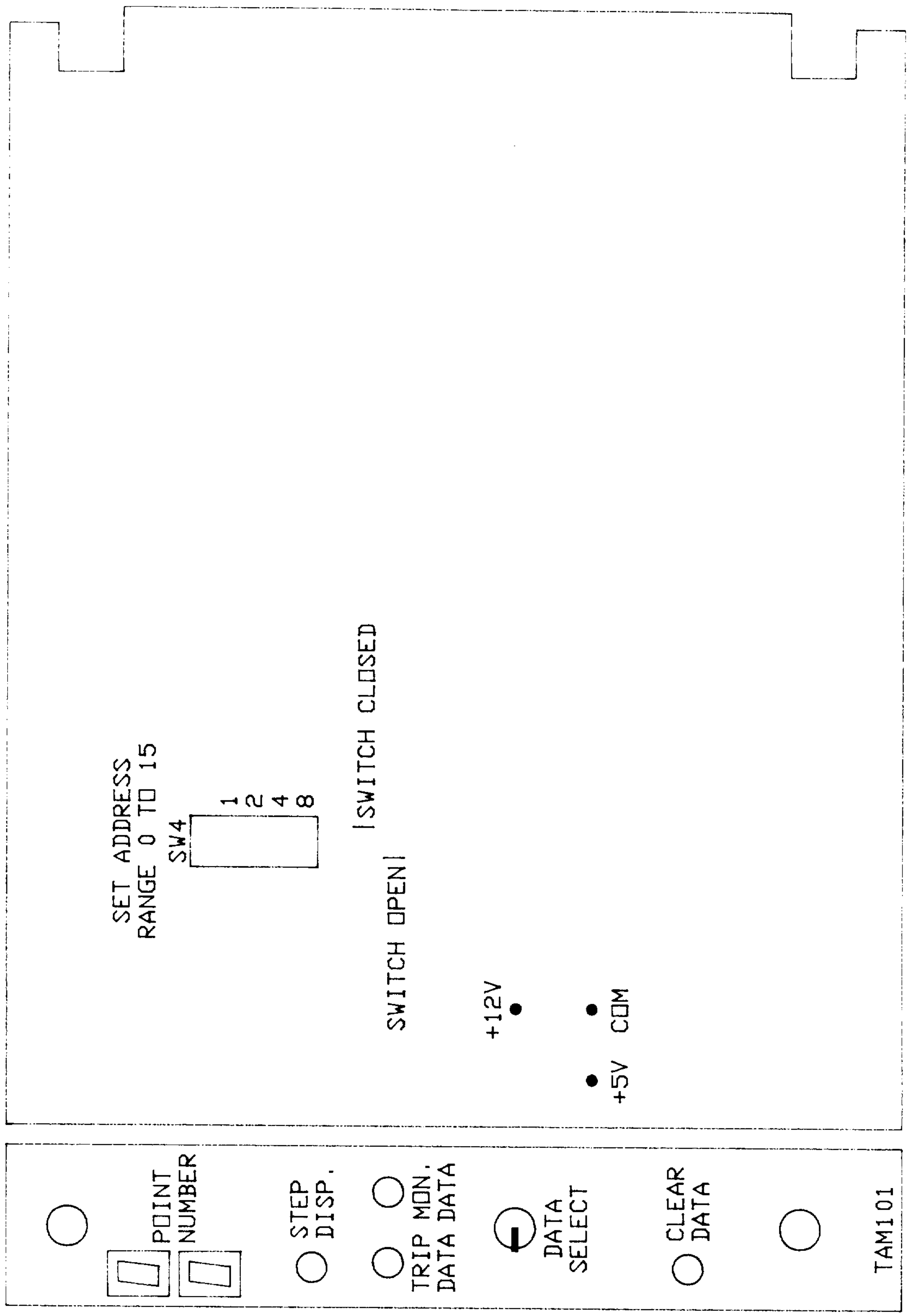


Figure MO-8 (0285A9831 [3]) TAM101

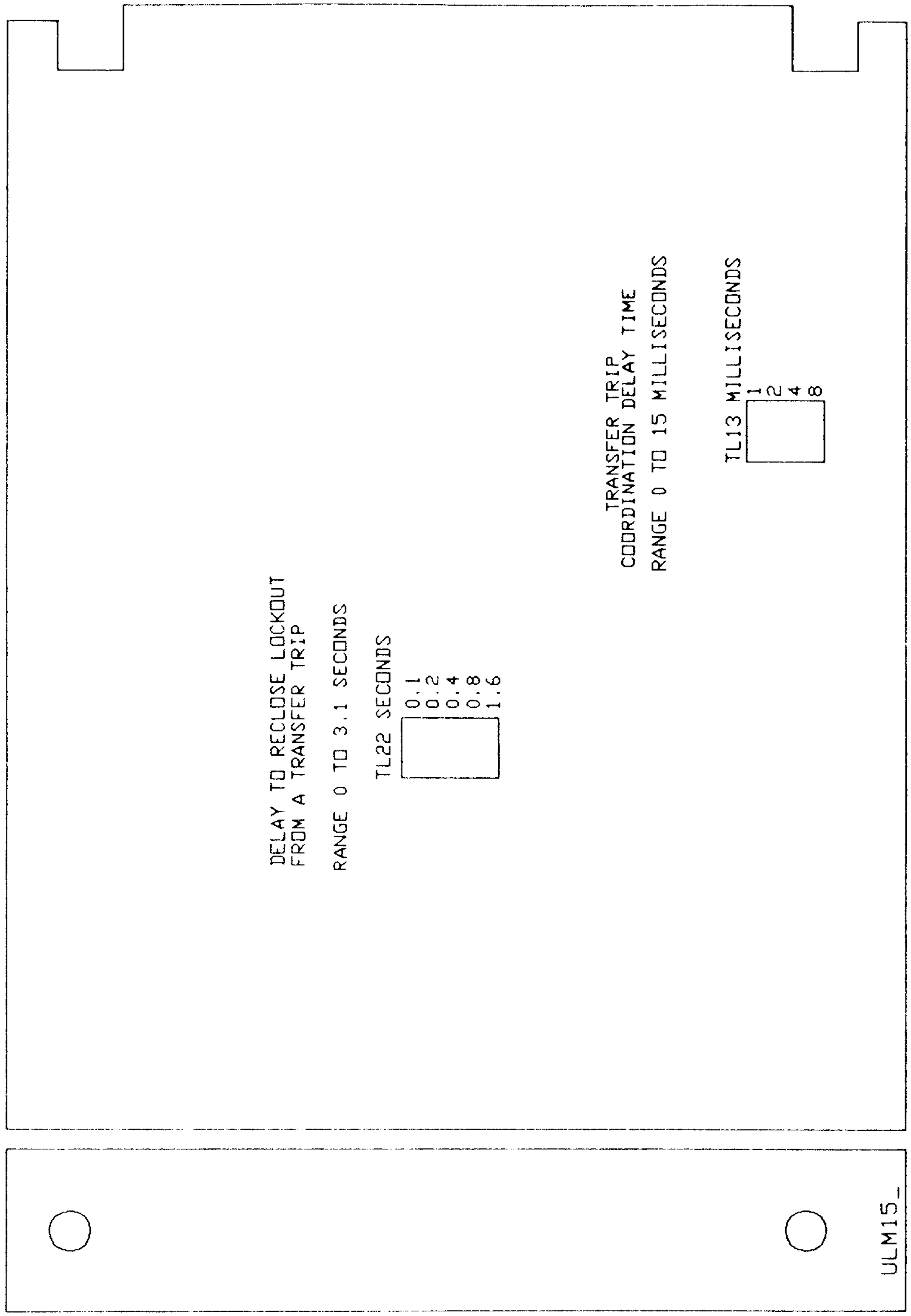


Figure MO-9 (0285A9832 [1]) ULM15-

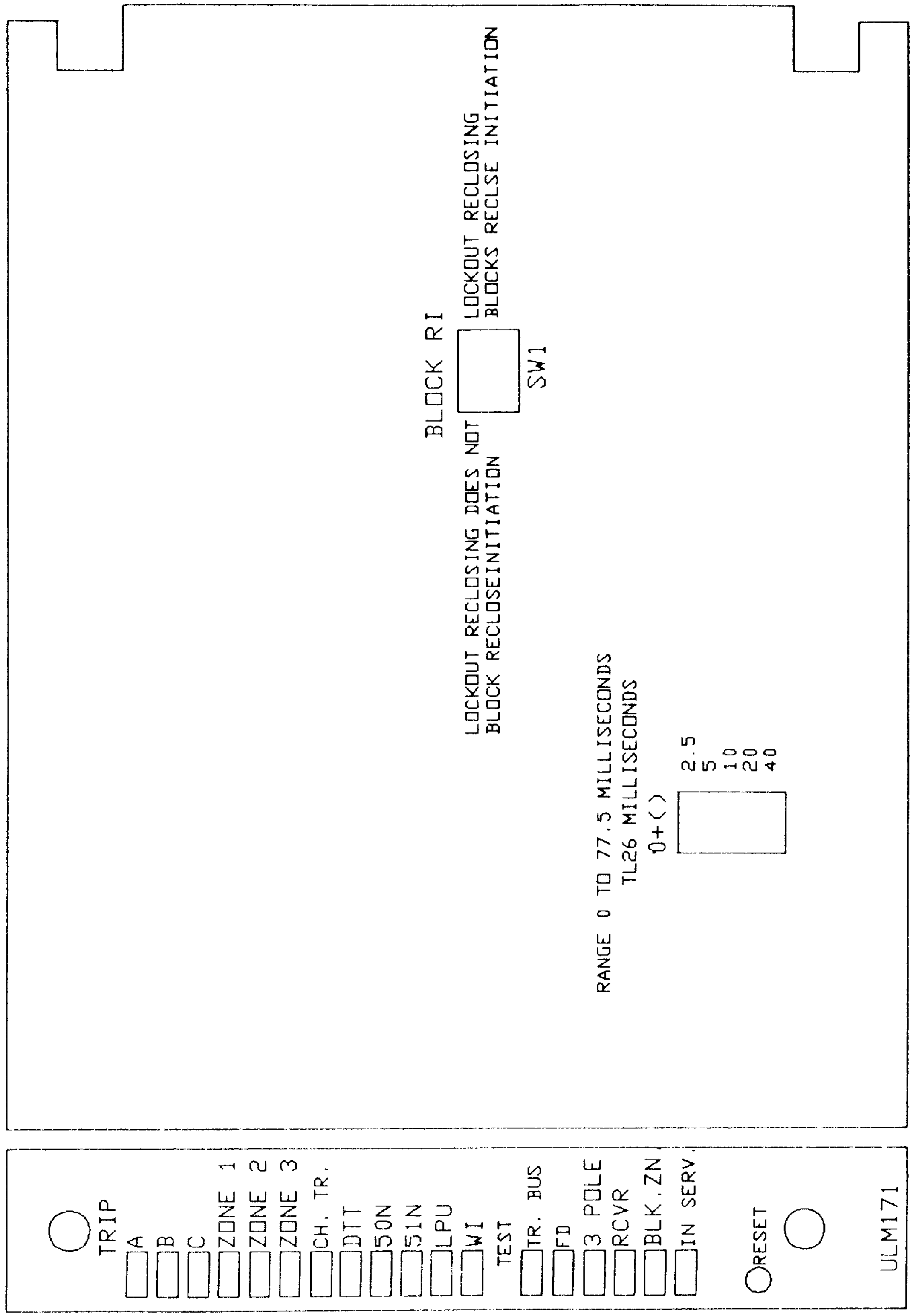


Figure MO-10 (0285A9833 [1]) ULM171

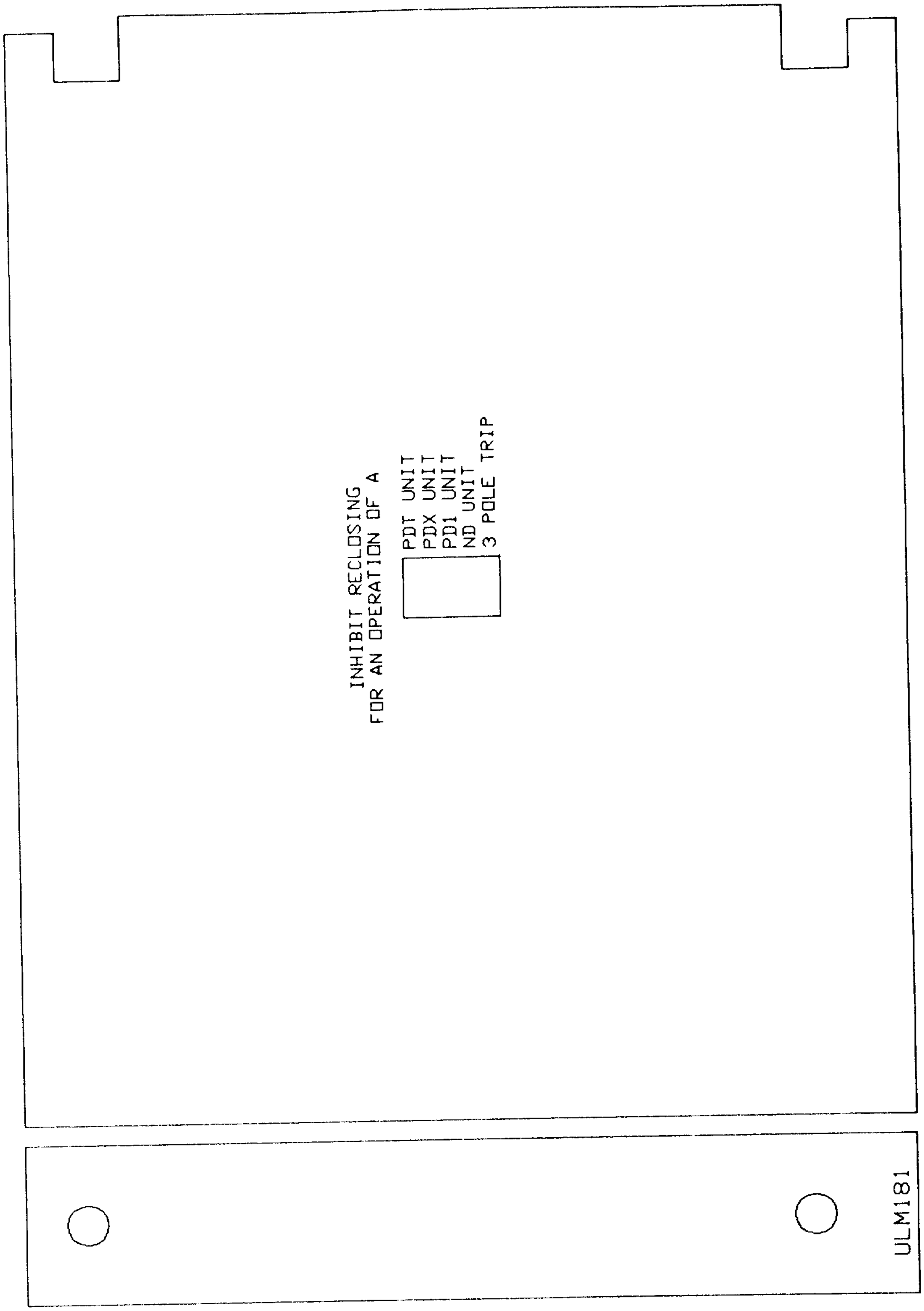


Figure MO-11 (0285A9834 [1]) ULM181

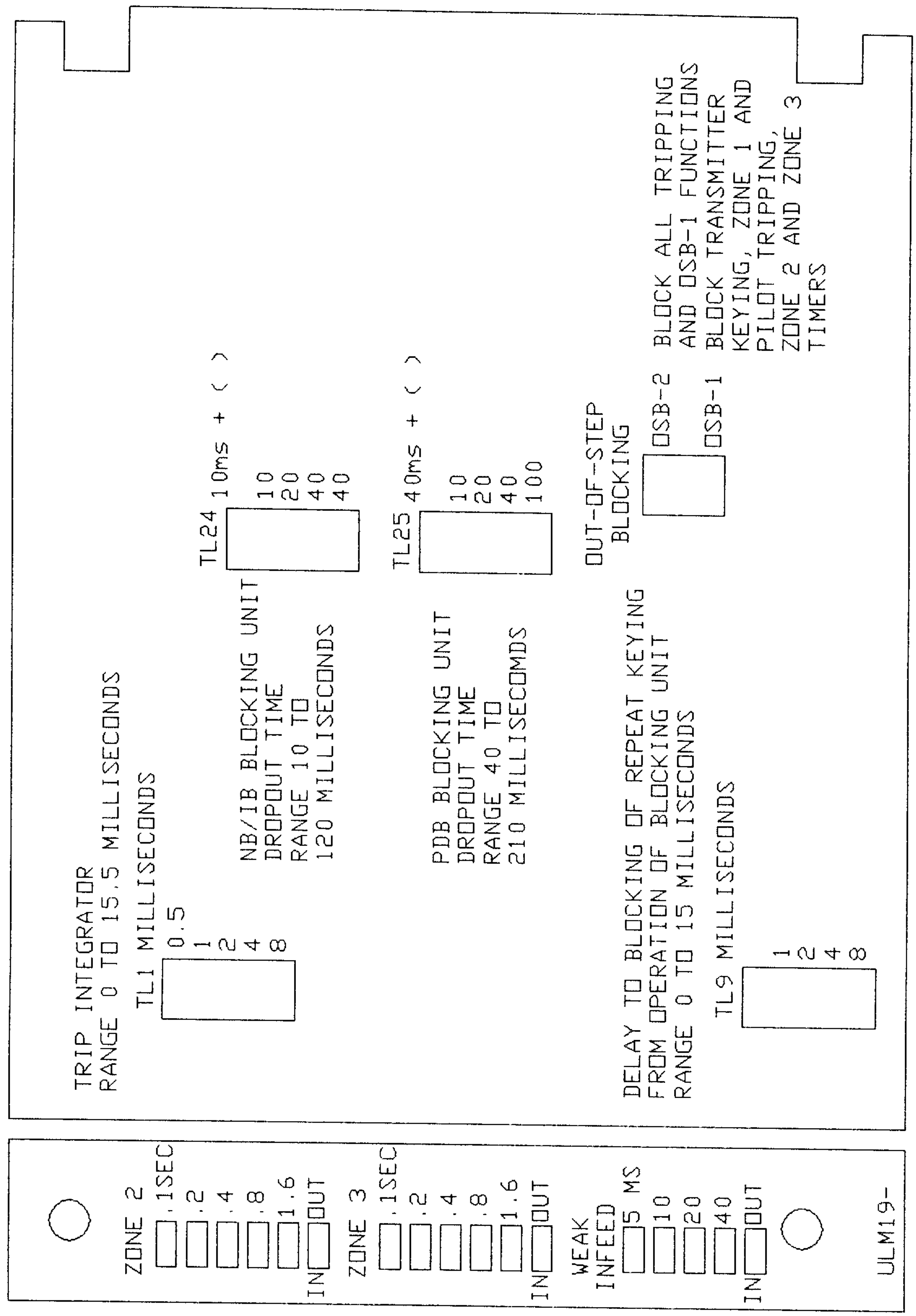


Figure MO-12 (0285A9835 [2]) ULM19-

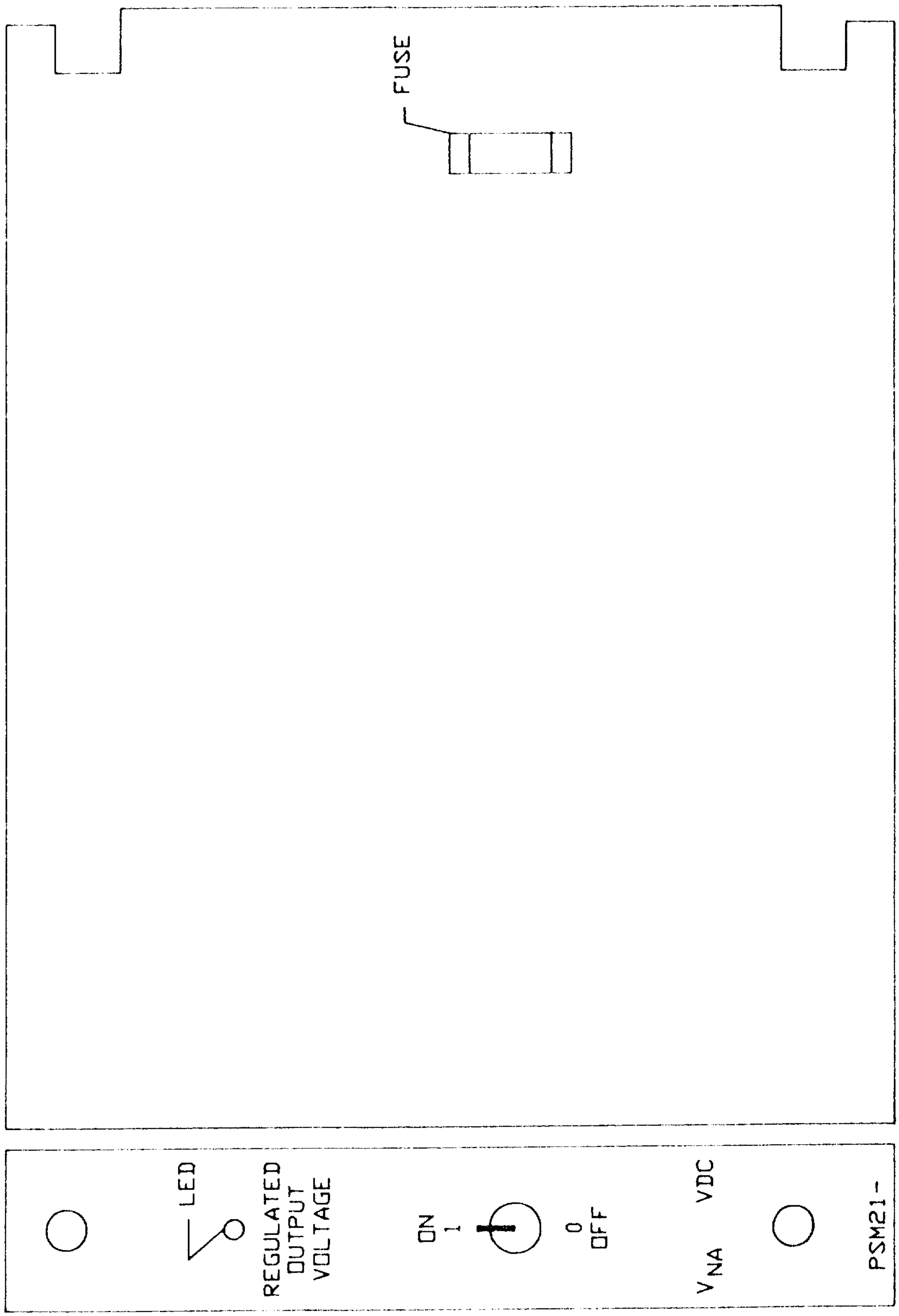


Figure MO-13 (0286A2547) PSM21-

Acceptance Tests

ACCEPTANCE TESTS

The operational tests described in this section should be conducted prior to the installation of the PLS system. These may be done on a "bench-top" basis.

One method of removing power is to turn OFF the power switch on the PSM21- power supply module and then remove both of the connection plugs located in the TPM position.

REQUIRED SETTINGS

To begin the acceptance tests, the module settings should be as indicated in Tables AT-1 and AT-2 (see next pages). Remove the modules to gain access to the links and switches referred to in Table AT-2. Module locations are shown in Figure MO-1.

Where there are different values for 5 ampere and 1 ampere relays, the value for the 1 ampere relay is given in parentheses after the 5-ampere value.

TEST EQUIPMENT

The acceptance tests may be conducted in a conventional manner using the following test equipment:

Three-phase source of voltage and current at rated frequency
DC control voltage source
Three AC voltmeters
Three AC ammeters
One oscilloscope
One card extender (GE #0138B7406G1)
One pair XTM test plugs (GE #XTM28R1 and XTM28L1)

The specific requirements for this equipment are given in the text of this **ACCEPTANCE TESTS** section, and in the associated test circuit diagrams.

The three-phase AC sinusoidal voltage must be balanced and undistorted. Similarly, the DC power should come from a good DC source having less than 5% ripple.

As an alternative, a three phase electronic test source may be used. In many cases, these devices enable the test circuits to be simplified considerably.

TEST CONNECTIONS

The test circuit diagrams indicate not only PLS terminal numbers (rear cover terminals) but also the corresponding XTM test plug terminal numbers, and Test Point connections. For the acceptance tests, the test connections should be made to the rear cover terminals. The test plugs are intended for post-installation testing and are described in a separate subsection under **PERIODIC TESTING.**

INITIAL RELAY SETTINGS

1. Place the front panel switches on the modules in the positions listed in Table AT-1. Refer to Module Section (MO) for switch locations.

Table AT-1: Front Panel Settings

Module	Function	Short Reach	Long Reach
DPM11-	Z1	3 (15)	12 (60)
DPM10-	ZT	2	2
ULM19-	ZONE 2	1 Sec	1 Sec
ULM19-	ZONE 3	3 Sec	3 Sec
ULM19-	WEAK INFEED	20 mSec	20 mSec

2. Place the internal links and switches on the modules in the positions shown in Table AT-2. Refer to Module Section (MO) for switch locations.

Table AT-2: Relay Settings

MODULE	FUNCTION	TYPE*	DESCRIPTION	SETTING
ADM10-	KT 0+()	5s	NT/NB compensation	0
	I2 shunt .01+()	5s	IT adaptive restraint	0.01
	I0 shunt .01+()	5s	IT adaptive restraint	0.01
	IT bias .05+()	5s	IT pickup setting	0.2
	IB bias .05+()	5s	IB pickup setting	0.2
AEM10-	IM .1+()	5s	IMA,IMB,IMC pickup	0.4
	3I0 .1+()	2s	3I0 Pickup	0.3
	PDX 1+()	4s	PDX reach multiplier	1.0
AEM11-	VA2 0+()	2s	NT/NB phase shift	0
	ZR1 70+()	2s	Replica impedance angle	85
	I1 .2+()	4s	I1T pickup	0.4
DNM10-	N2 1+()	4s	ND/NDD Z2 reach mult.	2.0
	N3 1+()	4s	ND/NDD Z3 reach mult.	4.0
	ND bias 0+()	6s**	ND restraint bias	0
DPM10-	OFFSET 0+()	2s	forward offset	0
	PDB 0.5+()	3s	PDB reach multiplier	1.0
	POSB 1.0+()	4s	POSB reach multiplier	1.0
	PDB TC	2b	PDB time constant	short
	PDT TC	2b	PDT time constant	short
	POSB TC	2b	POSB time constant	short
DPM11-	DT PU .4+()	6s	IDT pickup	0.4
	TOC PU .05+()	4s	ITOC pickup	0.2
	TD .5+()	5s	ITOC time dial	10.0
	PD1 bias 0+()	6s**	PD1 restraint bias	0
	K0 1+()	6s	IDT I0 compensation	1.0
	IDT K1	2b	IDT I1 restraint factor	1.0
	TOC K1	2b	ITOC I1 restraint factor	0.45
	IDT DIR	4b	IDT directional control	Non-Dir
	TOC DIR	3b	ITOC directional control	Non-Dir
ULM15-	TL13	4s	DTT timer	4msec
	TL22	5s	DTT reclose lockout timer	2sec
ULM171	BLOCK RI	1s	Reclose initiate control	Out/Left
	TL26	5s	Coordination timer	30msec
ULM181	Inhibit reclose	5s	PDT selection	Out/Left
			PDX selection	Out/Left
			PD1 selection	Out/Left
			ND selection	Out/Left
			3PT selection	Out/Left

MODULE	FUNCTION	TYPE*	DESCRIPTION	SETTING
ULM19-	TL1	5s	Trip integrator	3msec
	TL9	4s	Repeat blocking timer	4msec
	TL24	4s	NB dropout timer	80msec
	TL25	4s	PDB dropout timer	80msec
	OSB-1	2s	OSB block selection	Out/Left
	OSB-2	2s	OSB block selection	Out/Left

* 5s = five position toggle switch, 2b = two position berg post.
** Not adjustable on short reach models.

GENERAL INSTRUCTIONS

1. Remove the upper right blank module and insert a card extender (GE#0138B7406G1) in this location. The oscilloscope ground should be connected to pin 1 of this card for all tests.

   Place the test source in rated frequency position. Turn on the power supply and check that the green LED on the PSM21- module is lit.

2. The following tests are intended to verify the operation of the measuring units. If it is desired to check outputs or targets, refer to the logic diagram.

3. In the following tests, a LOW is defined as approximately 0 volts and a HIGH is defined as approximately 10 volts.

4. Where two numbers are shown: xx(yy), xx is the value to be used for relays rated 5 amperes, and (yy) is the value to be used for relays rated 1 ampere.

5. If the test source is an electronic type and one (or more) current source is not used for a particular test, that source must be set to "zero" in addition to being turned OFF. Also, these current sources should only be switched with the current set at, or near, zero.

6. All phase angles of test sources are shown relative to phase A voltage. A (+) phase angle refers to the referenced quantity leading phase A voltage. A (-) phase angle refers to the referenced quantity lagging voltage.

LEVEL DETECTOR TESTS

1. Make the connections shown in Figure AT-1 with relay input Y connected to BH1 or TP9. Connect the oscilloscope probe to card extender Pin 2. Set the oscilloscope for external trigger.

2. **Fault Detector Test**

   Set current IOP at 0.5 (0.1) ampere RMS. Close the push-button test switch for approximately one second. When the push button test switch opens, the oscilloscope trace at pin 2 should go to HIGH momentarily, after which it should return to LOW. Increase IOP to 2.25 (0.45) amperes RMS and repeat the test 2. The oscilloscope trace should remain HIGH except when the push-button test switch is closed.

3. **IT Test**

Move the oscilloscope input to card extender pin 14. Place a temporary jumper between pins 56 and 60 of the card extender. Set current IOP at 1.4 (0.28) amperes RMS. Close the push-button switch for approximately one second. When the push-button test switch opens, the oscilloscope trace should stay LOW.

Increase current IOP to 1.9 (0.38) amperes RMS and repeat the above test. The oscilloscope trace should go HIGH when the push-button test switch is open. Remove the temporary jumper between pins 56 and 60 on the card extender.

4. **IMA Test**

Make the connections shown in Figure AT-1 for testing the IMA function. Connect the scope probe to pin 3 of the test card extender. Slowly increase the current IOP until the oscilloscope trace goes from LOW to HIGH. At this point, the current should be between 1.96 (0.39) and 2.30 (0.46) amperes RMS.

5. **IMB Test**

Change connections to those shown in Figure AT-1 for testing the IMB function and repeat step 4. Monitor pin 4 on the oscilloscope.

6. **IMC Test**

Change connections to those shown in Figure AT-1 for testing the IMC function and repeat step 4. Monitor pin 5 on the oscilloscope.

7. **3I0 Test**

Change connections to those shown in Figure AT-1 for testing the 3I0 LD function. Slowly increase the current IOP until the oscilloscope trace at pin 10 goes from low to high. At this point the current should be between 1.47 (0.29) and 1.65 (0.33) amperes RMS.

8. **I1S Test**

Change connections to those shown in Figure AT-1 for testing the I1S function and repeat step 4, except that the pickup current should be between 0.60 (0.12) and 1.0 (0.2) amperes RMS. Monitor pin 11 on the oscilloscope.

9. **I1T Test**

Change connections to those shown in Figure AT-1 for testing the I1T function and repeat step 4, except that the pickup current should be between 5.56 (1.12) and 6.6 (1.32) amperes RMS. Monitor pin 12 on the oscilloscope.

10. **IB Test**

Place temporary jumpers between pins 55, 56 and 60 on the card extender. Connect the oscilloscope input to card extender pin No. 13. Slowly increase "IOP" until the oscilloscope trace goes from LOW to HIGH. At this pickup point, the current "IOP" should be between 0.9 (0.16) and 1.1 (0.22) amperes RMS.

11. **IDT Test**

Move the oscilloscope input to card extender pin No. 15 and repeat test 10, except that pickup should occur when "IOP" is between 2.70 (0.54) and 3.15 (0.63) amperes RMS.

12. **TOC PU Test**

Move the oscilloscope input to card extender pin No. 54 and repeat test 10, except that pickup should occur when "IOP" is between 1.1 (0.22) and 1.30 (0.26) amperes RMS.

13. **Not VA Test**

Change connections to those shown in Figure AT-2 for testing the "Not VA" function. Slowly decrease voltage "VA" until pulses start to appear on the oscilloscope. "VA" should be between 40 and 45 volts RMS at this point.
Continue decreasing "VA" until the oscilloscope trace is HIGH continuously, at which point "VA" should be 30 volts RMS or higher.

14. **Not VB Test**

Change connections to those shown in Figure AT-2 for testing the "Not VB" function. Repeat test 13.

15. **Not VC Test**

Change connections to those shown in Figure AT-2 for testing the "Not VC" function. Repeat test 13.

POSITIVE SEQUENCE DISTANCE TESTS

1. Change connections to those shown in Figure AT-3. Leave the temporary jumpers between pins 55, 56, and 60 on the card extender, and add a temporary jumper from pin 38 to pin 1. Move the oscilloscope input to card extender pin 17. Set angle IA = -85° (lagging), angle IB = +155° (leading) and angle IC = +35° (leading), at 5.0 (1.0) amperes RMS.

Long Reach Scheme Setup (PD1)

Set VA, VB and VC to 70 volts RMS and set angles VA to 0°, VB to -120° and VC to +120°. Reduce VA, VB, and VC until the measuring unit under test picks up as indicated by the oscilloscope trace going from LOW to HIGH.

Short Reach Scheme Setup (PD1)

Set VA, VB and VC to 60 volts RMS and set angles VA to 0°, VB to -120° and VC to +120°. Reduce VA, VB, and VC until the measuring unit under test picks up as indicated by the oscilloscope trace going from LOW to HIGH.

PD1 Reach

Move the oscilloscope input to card extender pin 17 perform the PD1 test as shown in the setup. This test checks the PD1 reach at the replica impedance angle including the pull-back effect at this current level (approximately 3%). See Table AT-3 for test tolerances.

PDX Reach

Move the oscilloscope input to card extender pin 19 and perform the test as shown in the setup. This test checks "PDX" reach at the replica impedance angle, including the pull-back effect at this current level (approximately 3%). See Table AT-3 for test tolerances.

PDT Reach

Reduce the reach on DPM11- module to 1 (5) ohms and increase the reach on the DPM10- module to 12 (60) ohms. Move the oscilloscope input to card extender pin 20 and perform the test as shown in the setup. See Table AT-3 for test tolerances. This test checks "PDT" reach at the replica impedance angle, including the pull-back effect at this current level (approximately 2%).

POSB Reach

Move the oscilloscope input to card extender pin 22 and lower IA, IB and IC to 4.5 (0.9) amperes RMS. Perform the test as shown in the setup. This test checks "POSB" reach. See Table AT-3 for test tolerances.

PDB Reach

Move the oscilloscope input to card extender pin 21 and raise IA, IB and IC to 5.0 (1.0) amperes RMS. Set angle IA = +95°, angle IB = -25° and angle IC = - 145°. Set VA, VB, and VC to 70 Volts RMS, at 0°, -120°, and +120° respectively. Set and lower the input voltages as shown in the setup until the oscilloscope trace goes from LOW to HIGH. See table III for test tolerances. Then raise the input voltages until the oscilloscope trace goes from HIGH to LOW. This dropout point should occur between 6 and 12 volts RMS above the pickup voltage.

TABLE AT-3: Reach Test Tolerances

UNIT	TP	SHORT REACH		LONG REACH	
		MIN	MAX	MIN	MAX
PD1	17	10	18	42	60
PDX	19	10	18	42	60
PDT	20	6	15	47	65
POSB	22	6	15	54	66
PDB	21	12	24	48	66

NEGATIVE SEQUENCE DISTANCE TESTS

ND

Change connections to those shown in Figure AT-4. Add temporary jumpers between pins 55, 56, 57, 58 and 60 on the card extender. Move the oscilloscope input to card extender pin 25. Increase the reach on DPM11- module to 3 (15) ohms. Set VA = 67 volts RMS, VB = 47 volts RMS and VC = 47 volts RMS. Set angle VB = -135° and angle VC = +135°. Set angle IOP = -175°. Slowly increase IOP until the oscilloscope trace goes from LOW to HIGH. At this pickup point, the current IOP should be between 10.5 (2.1) and 12.67 (2.53) amperes RMS. This test checks the "ND" reach, including the pull-back effect (approximately 6%).

ND Zone 2 Reach

Remove the temporary jumpers from pins 58 on the card extender. Repeat ND test, except that Iop at pin 25 should now be between 5.0 (1.0) and 7.0 (1.2) amperes RMS. This test checks the Zone 2 reach multiplier.

ND Zone 3 Reach

Remove the temporary jumper from pin 57 to pin 60 and add a temporary jumper from pin 58 to pin 60 on the card extender. Repeat ND Zone 2 Reach test, except that Iop at the pickup point should now be between 10.0 (2.0) and 14.0 (2.8) amperes RMS. This test checks the zone 3 reach multiplier.

NDD

Move the oscilloscope input to card extender pin No. 26 and repeat ND test, except that now the pickup should occur between 9.0 (1.80) and 13.0 (2.6) amperes. This test checks the "NDD" reach, including the pull-back effect (approximately 6%).

NDD Zone 2 Reach

Remove the temporary jumper from pin 58 to pin 60 on the card extender. Repeat ND test, except that Iop at pin 26 should now be between 5.1 (1.0) and 6.5 (1.1) amperes RMS. This test checks the Zone 2 reach multiplier.

NDD Zone 3 Reach

Remove the temporary jumper from pin 57 to pin 60 and add a temporary jumper from pin 58 to pin 60 on the card extender. Repeat ND Zone 2 Reach test, except that Iop at the pickup point should now be between 10.0 (2.0) and 14.0 (2.8) amperes RMS. This test checks the zone 3 reach multiplier.

NEGATIVE SEQUENCE DIRECTIONAL TESTS

1. **NT** Unit.

   Change connections to those shown in Figure AT-5 with relay input Y connected to BH1 or TP9. Move the oscilloscope input to card extender pin No. 23. Set VA = 30 volts RMS, VB = 67 volts RMS, VC = 67 volts RMS. Set angle VB = -120° and angle VC = +120°. Set angle IA = -85°. Slowly increase IA until the oscilloscope trace goes from LOW to HIGH. At this pickup point, current IA should be less than 0.05 (0.01) amperes RMS.

   Change angle IA to +95° and check that the oscilloscope trace does not go HIGH as IA is increased up to 10 (2) amperes RMS.

2. **NB** Unit.

   Move the oscilloscope input to card extender pin No. 24. Reduce IA to 1.0 (0.2) amperes RMS and check that the oscilloscope trace is HIGH.

   Change the angle IA to -85° and check that the oscilloscope trace is LOW.

PHASE SELECTORS

1. Move the oscilloscope input to card extender pin 27. Set IOP = 1.6 (0.32) amperes RMS and leave all other settings set per step 1 of NEGATIVE-SEQUENCE DIRECTIONAL TESTS. Check that the oscilloscope trace is HIGH.

2. Change connections to those shown for testing PHB SEL in Figure AT-5. Raise VA to 67 volts RMS, lower VB to 30 volts RMS and set angle IOP to -205°. Check that the oscilloscope trace at pin 28 is HIGH.

3. Change connections to those shown for testing PHC SEL in Figure AT-5. Raise VB to 67 volts RMS, lower VC to 30 volts RMS and set angle of Iop to -325°. Check that the oscilloscope trace at pin 29 is HIGH.

DIELECTRIC TESTS

Dielectric testing may be performed 1) between all terminals (tied together) and the case, and 2) between independent circuit groups (refer to elementary diagram, Figure SD-4). The recommended voltage is 2000 volts RMS for initial testing and 1500 volts RMS for subsequent periodic testing. The test voltage should be applied for 1 minute.

CAUTION

When hipot testing, it is necessary to remove the jumpers between terminals BH13 and BH14. This removes the grounding connection between the surge capacitors and caseground. Failure to do so could result in damage to the filter capacitors on the PSM module when the DC supply terminals are tested.

NOTE

All other studs can be tested with the jumper in place without damage; however, leakage will be indicated due to current flowing through the surge capacitors.

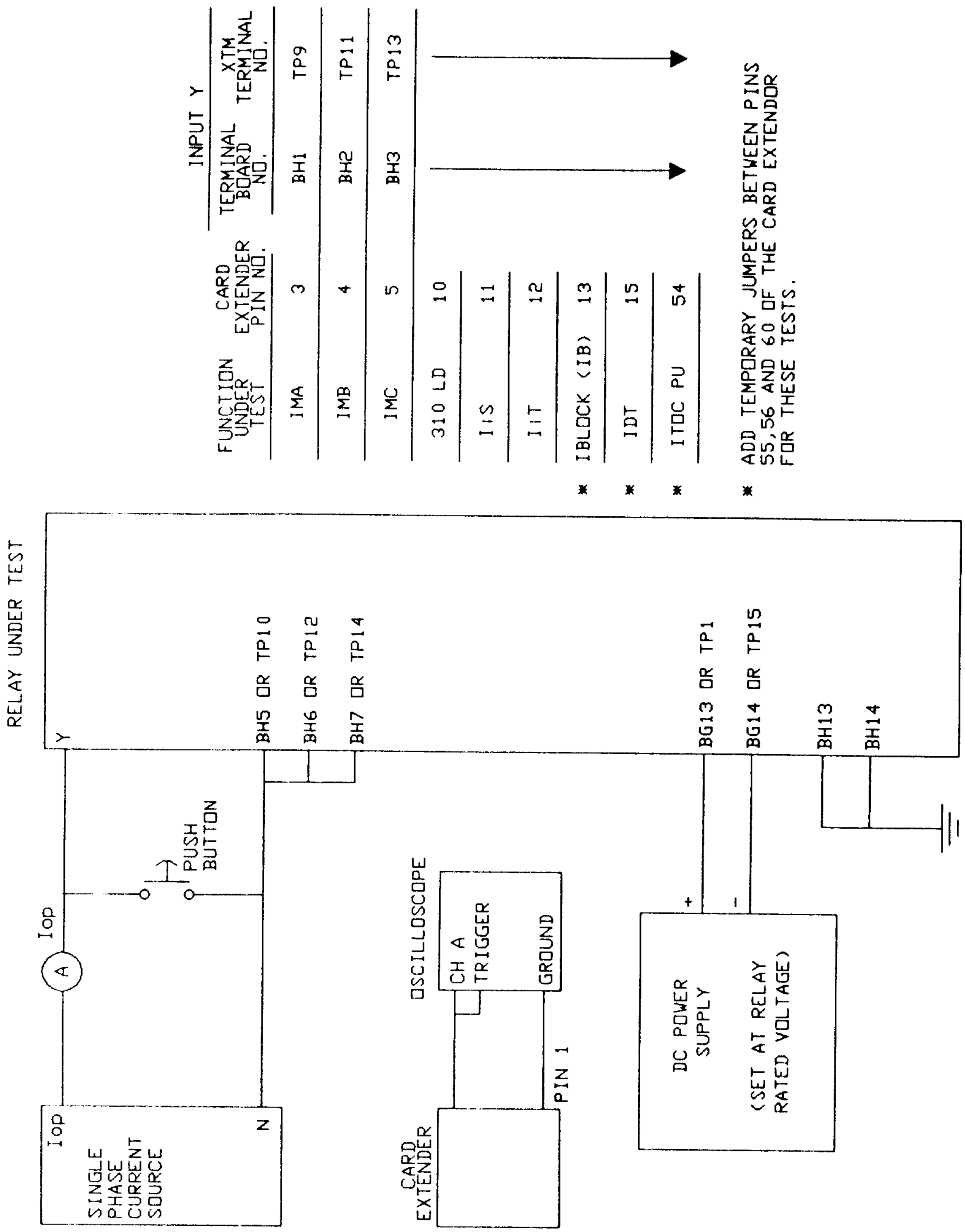


Figure AT-1 (0285A9838 [1]) Level Detector Test Connections

FUNCTION UNDER TEST	CARD EXTENDER PIN NO.	INPUT Y TERMINAL BOARD NO.	INPUT Y XTM TERMINAL NO.
NOT VA	6	BG2	TP25
NOT VB	7	BG3	TP26
NOT VC	8	BG4	TP27

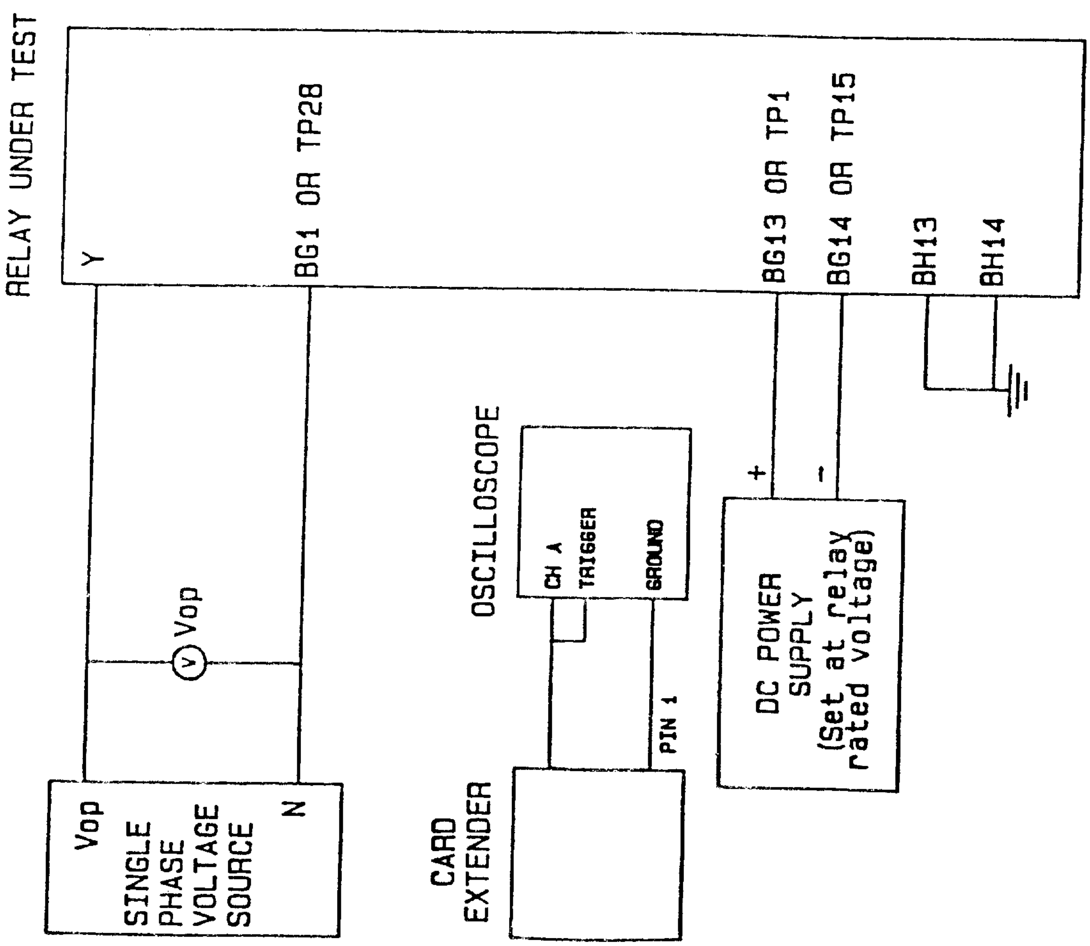


Figure AT-2 (0285A9839 [1]) Not VA, VB, VC Test Connections

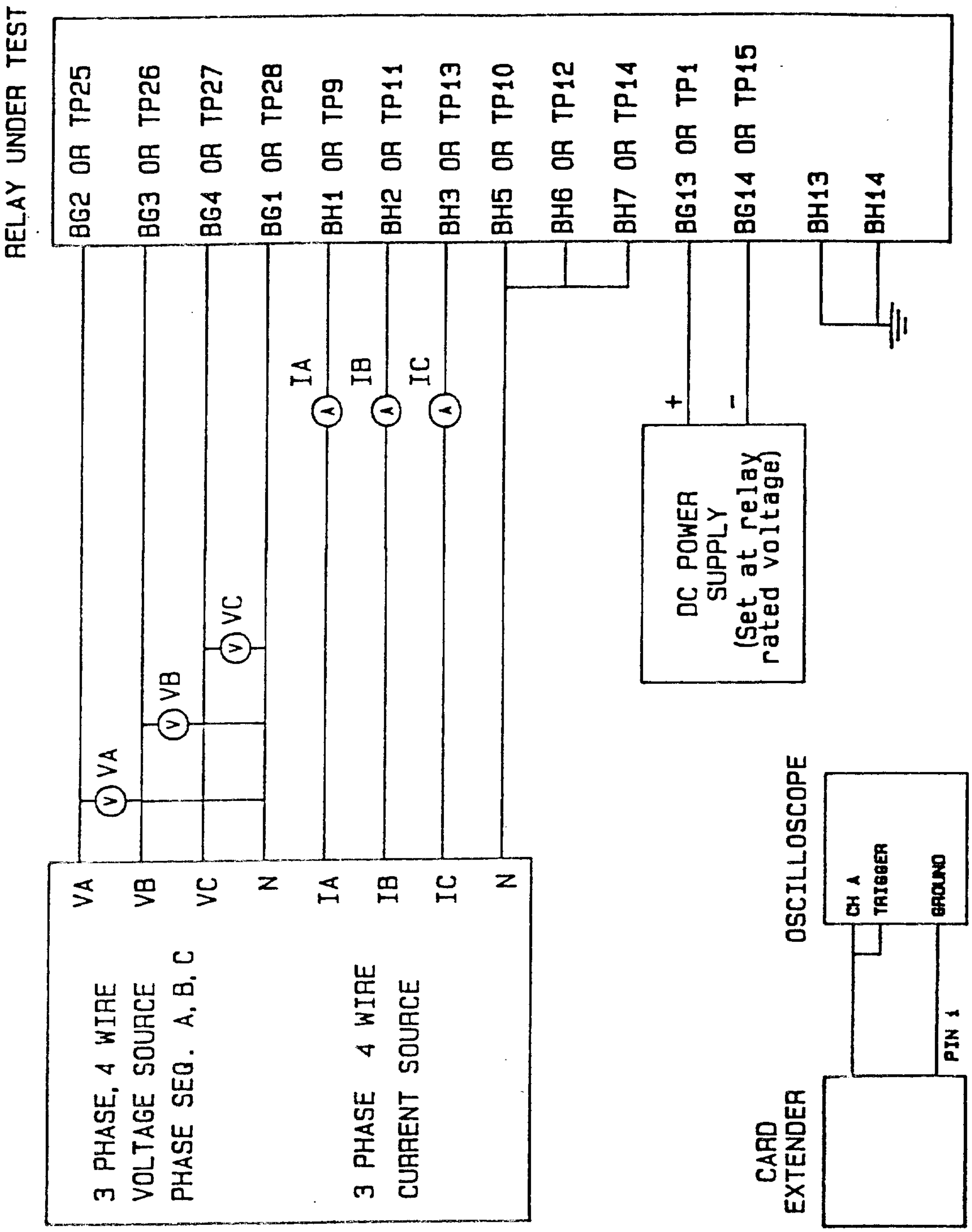


Figure AT-3 (0285A9840 [1]) Positive-Sequence Distance Test Connections

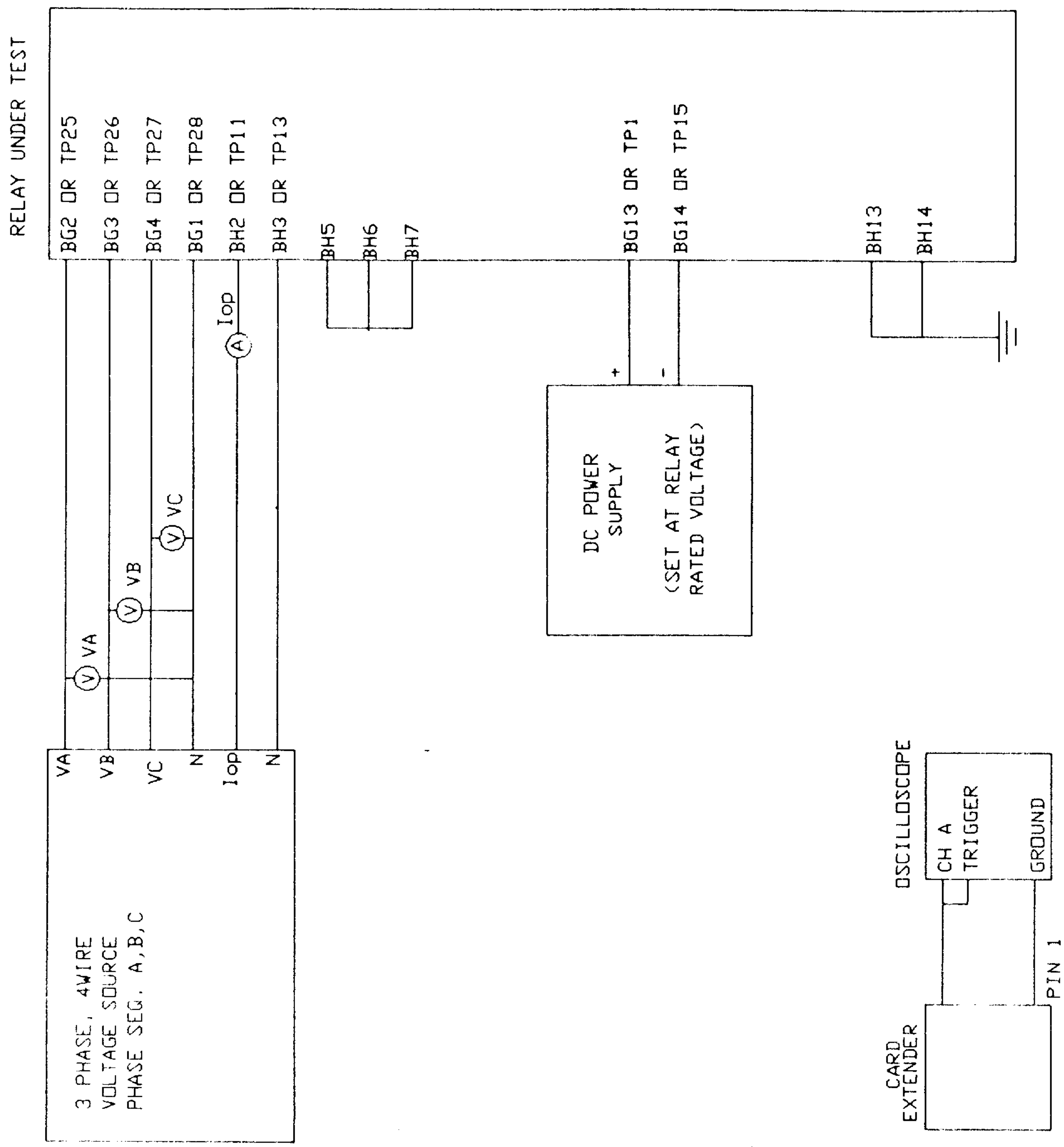


Figure AT-4 (0285A9841 [2]) Negative-Sequence Distance Test Connections

FUNCTION UNDER TEST	CARD EXTENDER PIN NO.	INPUT Y TERMINAL BOARD NO.	INPUT Y XTM TERMINAL NO.
PH A SEL	27	BH1	TP9
PH B SEL	28	BH2	TP11
PH C SEL	29	BH3	TP13

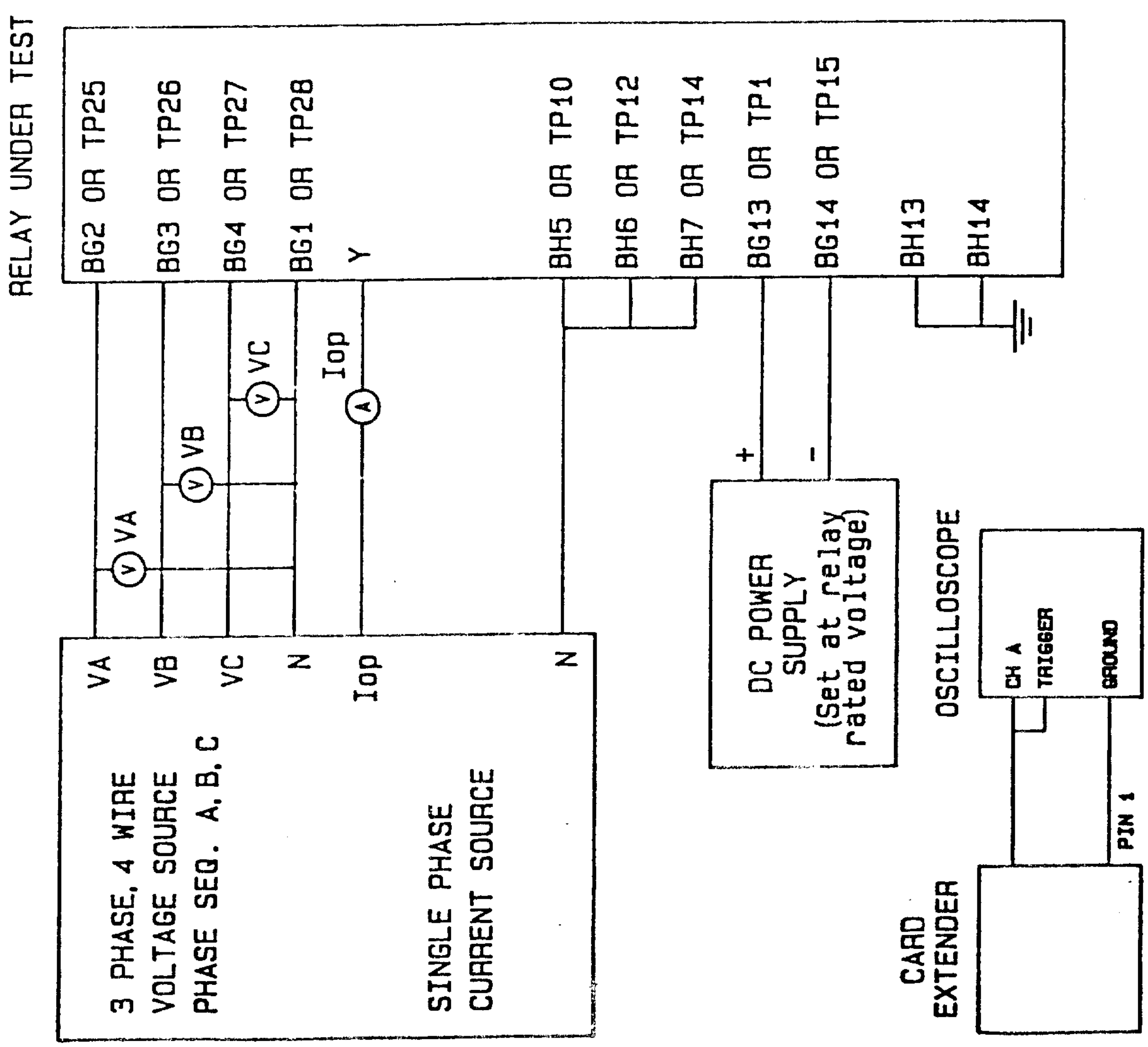


Figure AT-5 (0285A9842 [1]) Negative-Sequence Directional Test Connections and Phase Selectors Test Connections

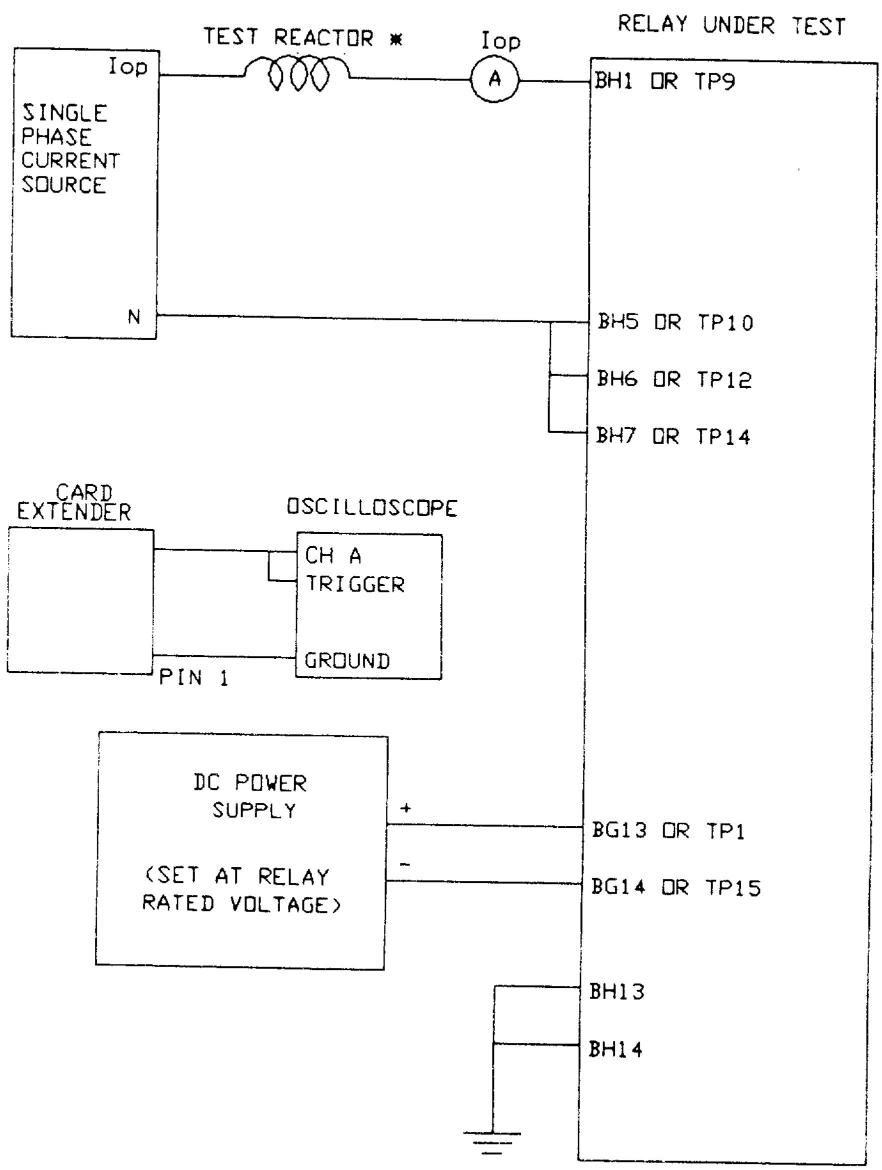


Figure AT-6 (0285A9843 [1]) IT Test Connections

Periodic Tests

PERIODIC TESTING

TESTING THE PLS OPERATION WITH DIFFERENT SETTINGS

Because of the level of sophistication of the PLS modular relay system and the large number of selections that may be made, it is impossible to present one or two equations that will satisfy every condition. An attempt has been made, however, to allow the calculation of the pickup currents or voltages for the functions when using the test circuits described in the corresponding section of the ACCEPTANCE TESTS portion of this instruction book. This will permit some testing to be done using settings other than those specified as part of the acceptance tests.

To test with different settings, refer to the corresponding section of ACCEPTANCE TESTS. For instance, if the PD1 function is being tested, use the same test setup and settings as described in the PD1 portion, but use the equations and notes below to modify the expected test results.

Tolerance

The tolerances on the pickup values calculated for the PLS functions are dependent on the magnitude of the test current, as listed in Table PT-1.

TABLE PT-1: Test Tolerances*

ITEST (RMS Amperes)		Tolerance in Percent	
IN=5	IN=1	Minimum	Maximum
0-1	0 -0.2	0	+15
1-3	0.2-0.6	-2	+10
3-7	0.6-1.4	-3	+7
>7**	>1.4**	-5	+5

* The actual pickup current should be within the tolerance given in Table PT-1 for the particular value of test current, or ±.025 per unit of IN, whichever is greater.

** Note that the relay is continuously rated for 10 (2) amperes RMS. For test currents greater than the continuous rating, testing should be conducted with a duty cycle. For example, with a test current of 20 (4) amperes, the current should not be applied longer than 5 minutes, followed by a cooling-off period of 5 minutes.

CURRENT LEVEL DETECTORS

A. IMA, IMB, IMC

Use the connections shown in Figure AT-1 for testing IMA. Slowly increase the current, IOP, until the oscilloscope trace goes from LOW to HIGH. The nominal pickup current is given by Equation 1. The actual pickup current should be within the tolerance given in Table PT-1 for the particular value of test current.

$$IPU = IM \times IN \qquad (1)$$

Where: IM is the pickup set on the AEM10- module
IN is the rated relay current (1 or 5 amperes)
IPU is the nominal pickup current

To test IMB and IMC use the procedure specified for IMA, and the appropriate connections from Figure AT-1.

B. **3I0**

Use the connections shown in Figure AT-1 for testing 3I0. Slowly increase the current, IOP, until the oscilloscope trace goes from LOW to HIGH. The nominal pickup current is given by Equation 2. The actual pickup current should be within the tolerance given in Table PT-1 for the particular value of test current, or $\pm$.025 per unit, whichever is greater.

$$IPU = 3I0 \times IN \qquad (2)$$

Where: 3I0 is the pickup set on the AEM10- module
IN is the rated relay current (1 or 5 amperes)
IPU is the nominal pickup current

C. **I1T**

Use the connections shown in Figure AT-1 for testing I1T. Slowly increase the current, IOP, until the oscilloscope trace goes from LOW to HIGH. The nominal pickup current is given by Equation 3. The actual pickup current should be within the tolerance given in Table PT-1 for the particular value of test current.

$$IPU = I1 \times IN \times 3 \qquad (3)$$

Where: I1 is the pickup set on the AEM11- module
IN is the rated relay current (1 or 5 amperes)
IPU is the nominal pickup current

D. **IB**

Place temporary jumpers between pins 55, 56, and 60 on the test card extender. Use the connections shown in Figure AT-1 for testing IB. Slowly increase current IOP until the oscilloscope trace goes from LOW to HIGH. The nominal pickup current is given by Equation 4. The actual pickup current should be within the tolerance given in Table PT-1 for the particular value of test current.

$$IPU = 1.07 \times IB\ BIAS \times IN \qquad (4)$$

Where: IB BIAS is the IB pickup set on the ADM10- module
IN is the rated relay current (1 or 5 amperes)
IPU is the nominal pickup current
Tolerance = $\pm$.025 per unit, or equal to Table PT-1, whichever is greater

E. **IT**

The IT unit in the PLS is designed with an adaptive pickup circuit; that is, when a current higher than pickup is suddenly applied to the relay, IT will pick up initially, but after a time delay the unit will "adapt" to the steady-state current level and will reset. The duration of the output is a function of the difference between the applied current and the pickup current.

There are two methods of testing the IT unit. The first involves defeating the adaptive pickup circuit by means of a temporary jumper. This allows the pickup to be measured with steady-state currents. The second method uses a transiently applied test current. In this test, the IT unit will "adapt" and drop out after a short time delay.

Method I (without adaptive pickup)

Place the ADM10- module in a card extender. Connect a jumper from TP7 on the module (TP7 is located behind the nameplate, towards the bottom of the module) and reference (pin 1 on the card extender).

Place temporary jumpers between pins 55, 56, and 60 on a second card extender in the test card position. Use the test connections shown in Figure AT-6 and connect the oscilloscope input to test card extender pin 14. Slowly increase current IOP until the oscilloscope trace goes from LOW to HIGH. The nominal pickup current is calculated in Equation 5. The actual pickup current should be within the tolerance given in Table PT-1 for the particular value of test current.

$$IPU = 1.1 \times IT\ BIAS \times IN \qquad (5)$$

Where: IT BIAS is the IT pickup set on the ADM10- module
IN is the rated relay current (1 or 5 amperes)
IPU is the nominal pickup current

After the IT unit has picked up, remove the jumper from TP7 and check that the oscilloscope trace goes from HIGH to LOW. Place the ADM10- module in its original location.

Method II (with adaptive pickup)

NOTE: When the PLS is tested with transiently-applied current, the waveform of the test current should be similar to the currents the relay will see in service. In particular, the relay should not be tested with currents that have an unrealistic rate of rise. Therefore, the test current should be limited by reactance, rather than by resistance. If an electronic current source is used, it should be the type that only turns ON the current at a current zero crossing. Use of other types of current sources may cause pickup values that appear to be out of tolerance.

Place temporary jumpers between pins 55, 56, and 60 on the card extender in the test position. Connect the oscilloscope input to pin 14 on the test card extender. Use the test current connections of Figure AT-6.

Without current applied to the relay, set the current level to the value specified by Equation 6.

$$IPU = 1.4 \times IT\ BIAS \times IN \qquad (6)$$

Where: IT BIAS is the IT pickup set on the ADM10- module
IN is the rated relay current (1 or 5 amperes)
IPU is the nominal pickup current

Suddenly apply the calculated test current and check that the oscilloscope trace momentarily goes from LOW to HIGH. If this test is repeated, wait at least 30 seconds between tests to allow the adaptive circuit to reset.

Without current applied to the relay, set the current level to the value specified by Equation 7.

$$IPU = 1.3 \times IT\ BIAS \times IN \qquad (7)$$

Where: IT BIAS is the IT pickup set on the ADM10- module
IN is the rated relay current (1 or 5 amperes)
IPU is the nominal pickup current

Suddenly apply the calculated test current and check that the oscilloscope trace does not go from LOW to HIGH.

F. **Fault Detector Pickup.**

Set current IOP at 0.5 (0.1) ampere RMS. Close the pushbutton test switch for approximately one second. When the push button test switch opens, the oscilloscope trace at pin 2 should go to HIGH momentarily, after which it should return to LOW. Increase IOP to 2.25 (0.45) amperes RMS and repeat the test. The oscilloscope trace should remain HIGH except when the pushbutton test switch is closed.

DIRECTIONAL TESTS

NOTE: The IDT and ITOC tests can be performed directionally, or non-directionally, depending upon customer settings. If both tests are performed, return the directional controls to the proper setting.

A. **ITOC** (Non-directional)

Use the connections shown in Figure AT-1 for testing TOC. Set the TOC DIR setting to NON-DIR on the DPM11- module for this test. Return the ITOC pickup setting to required value. Slowly increase the current, IOP, until the oscilloscope trace goes from LOW to HIGH. The nominal pickup current is given by Equation 8. The actual pickup current should be within the tolerance given in Table PT-1 for the particular value of test current.

$$IPU = \frac{3}{3\text{-}TOC\ K1} \times \quad TOC\ PU \times IN \qquad (8)$$

Where: TOC PU is the pickup set on the DPM11- module
TOC K1 is the I1 restraint factor set on the DPM11- module (0 or 0.45)
IN is the rated relay current (1 or 5 amperes)
IPU is the nominal pickup current

NOTE: Return the TOC DIR setting to its required setting following this test.

B. **ITOC** (Directional)

Use the connections shown in Figure AT-5, and connect "Y" to BH1. Set the IDT DIR berg post to DIR on the DPM11- module. Place temporary jumpers between pins 55, 56, and 60 on the test card extender. The nominal pickup current is given by equation 4. The actual pickup current should be within the tolerance given in Table PT-1 for the particular value of test current.

Set the voltage phase angles per Table PT-2, set IOP to -85°. Set VA to 47V, VB and VC to 69 volts RMS.

Slowly increase Iop from 0 amps until the oscilloscope trace at pin 16 goes from LOW to HIGH.

Change the angle of IOP to +100° and verify that the oscilloscope trace goes from HIGH to LOW.

C. **IDT** (Non-directional)

NOTE: To prevent ITOC tripping during this test, temporarily set ITOC pickup to the maximum value and the time dial to ten (10). If the IDT directional control is set to "NON-DIR" go to test E and continue testing.

Use the connections shown in Figure AT-1 for testing IDT. Place temporary jumpers between pins 55,56, and 60 on the test card extender. Slowly increase the current, IOP, until the oscilloscope trace goes from LOW to HIGH. The nominal pickup current is given by Equation 9. The actual pickup current should be within the tolerance given in Table PT-1 for the particular value of test current.

$$IPU = \frac{3}{3\text{-}IDT\ K1} \times DT\ PU \times IN \qquad (9)$$

Where: DT PU is the pickup set on the DPM11- module
IDT K1 is the I1 restraint factor set on the DPM11- module (0 or 1)
IN is the rated relay current (1 or 5 amperes)
IPU is the nominal pickup current

D. **IDT** (Directional)

Use the connections shown in Figure AT-5, and connect "Y" to BH1. Set the IDT DIR berg post to DIR on the DPM11- module. Place temporary jumpers between pins 55,56, and 60 on the test card extender. The nominal pickup current is given by equation 4. The actual pickup current should be within the tolerance given in Table PT-1 for the particular value of test current.

Set the voltage phase angles per Table PT-2, set IOP to -85°. Set VA to 47V, VB and VC to 69 volts RMS.

Slowly decrease Iop from 2 amps until the oscilloscope trace at pin 15 goes from HIGH to LOW.

Change the angle of IA to +100° and verify that the oscilloscope trace goes from LOW to HIGH.

POSITIVE-SEQUENCE DISTANCE UNITS

A. **PD1**

Use the connections shown in Figure AT-3, and connect a temporary jumper between pin 38 and pin 1. Connect temporary jumpers between pins 55, 56 and 60 on a test card extender in the test card position. Connect the oscilloscope input to pin 17 on the test extender. For the PD1 test only, set the "ZT" reach on the front plate of the DPM10- module to 2 (10) ohms.

Set the current and voltage phase angles per Table PT-2.

TABLE PT-2: Phase Angle Settings

FUNCTION	ANGLE
IA	-θ
IB	-(θ + 120)
IC	120-θ
VA	0
VB	-120
VC	120

Where is the ZR1 angle set on the AEM11- module.

The current used for this test should be equal to or greater than the value given in Table PT-3. The magnitude of all three phase currents should be equal.

TABLE PT-3: Test Tolerance

Z1	ITEST	TOLERANCE (%) MIN	TOLERANCE (%) MAX	Z1	ITEST
1 - 6Ω	10	-5	+5	5 - 30Ω	2
6 - 12Ω	5	-7	+3	30 - 60Ω	1
12 - 20Ω	3	-10	+2	60 - 100Ω	0.6
20 - 25Ω	2	-15	0	100 - 150Ω	0.4

The nominal operating voltage is given by Equation 10.

$$VOP = (ITEST \times Z1) - PD1\ BIAS - 1.5 \qquad (10)$$

Where: ITEST is the test current
Z1 is the PD1 reach set on the front panel of the DPM11- module
PD1 BIAS is the bias set on the DPM11- module multiplied by 67 to convert from per unit
VOP is the nominal operating voltage

The applied voltage should initially be set to a value larger than the nominal operating voltage, and the three phase voltages should be lowered simultaneously until the PD1 unit operates, i.e. until pin 17 on the test extender steps from LOW TO HIGH. The actual operating voltage should be within the tolerances given in Table PT-3 for the value of ITEST used.

B. **PDT**

Use the connections shown in Figure AT-3. Connect temporary jumpers between pins 55, 56, and 60 on a test card extender in the test card position. Connect the oscilloscope input to pin 20 on the test extender.

Set the current and voltage phase angles per Table PT-2.

The current used for this test should be equal to or greater than the value given in Table PT-4. The magnitude of all three phase currents should be equal.

TABLE PT-4: Test Tolerances

IN = 5 ZT	ITEST	Tolerance% MIN	MAX	IN = 1 ZT	ITEST
2- 6Ω	10	5	5	10- 30Ω	2
6-12Ω	5	7	3	30- 60Ω	1
12-20Ω	3	10	2	60-100Ω	0.6
20-30Ω	2	15	0	100-150Ω	0.4
30-40Ω	1.5	15	0	150-200Ω	0.3
40-60Ω	1	15	0	200-30Ω	0.2

The nominal operating voltage is given by Equation 11.

$$VOP = ITEST \times ZT \qquad (11)$$

Where: ITEST is the applied test current
ZT is the PDT reach set on the front panel of the DPM10- module
VOP is the nominal operating voltage

The applied voltage should initially be set to a value larger than the nominal operating voltage, and the three phase voltages should be lowered simultaneously until the PDT unit operates, i.e. until pin 20 on the test extender steps from LOW TO HIGH. The actual operating voltage should be within the tolerances given in Table PT-4 for the value of ITEST used.

C. **PDB**

Use the connections shown in Figure AT-3. Connect temporary jumpers between pins 55, 56, and 60 on a test card extender in the test card position. Connect the oscilloscope input to pin 21 on the test extender.

Set the current and voltage phase angles per Table PT-5. The reach of the PDB unit is equal to the product of the PDT reach and the PDB reach multiplier set on the DPM10-. The recommended test current is determined by the PDB reach, as shown in Table PT-6. The current used for this test should be equal to or greater than the value given in Table PT-6. The magnitude of all three phase currents should be equal.

TABLE PT-5: Voltage/Current Settings

Function	Phase Angle
IA	180-θ
IB	-(θ-60)
IC	-(θ+60)
VA	0
VB	-120
VC	+120

Where   is the ZR1 angle set on the AEM11- module.

TABLE PT-6: PDB Test Current Values

IN=5 ZRPDB	IN=5 ITEST	IN=1 ZRPDB	IN=1 ITEST
2- 6	10	10- 30	2
6-12	5	30- 60	1
12-20	3	60-100	0.6
20-30	2	100-150	0.4
30-40	1.5	150-200	0.3
40-60	1	200-300	0.2

The nominal operating voltage is given by Equation 12.

$$VOP = ITEST \times ZRPDB \qquad (12)$$

Where: ITEST is the applied test current
ZRPDB = ZT x PDB
ZT is the PDT reach set on the front of the DPM10- module.
PDB is the reach multiplier, set on the DPM10- module.
VOP is the nominal operating voltage

The applied voltage should initially be set to a value larger than the nominal operating voltage, and the three phase voltages should be lowered simultaneously until the PDB unit operates, i.e. until pin 21 on the test extender steps from LOW TO HIGH. The actual operating voltage should be within the tolerances given in Table PT-3 for the value of ITEST used.

D. **POSB**

Use the connections shown in Figure AT-3. Connect temporary jumpers between pins 55, 56, and 60 on a test card extender in the test card position. Connect the oscilloscope input to pin 22 on the test extender.

Set the current and voltage phase angles per Table PT-2. The reach of the POSB unit is equal to the product of the PDT reach and the POSB reach multiplier set on the DPM10-. The recommended test current is determined by the POSB reach, as shown in Table PT-7. The current used for this test should be equal to or greater than the value given in Table PT-7. The magnitude of all three phase currents should be equal.

TABLE PT-7: POSB Test Current Values

IN=5 ZRPOSB	IN=5 ITEST	IN=1 ZRPOSB	IN=1 ITEST
2- 6	10	10- 30	2
6-12	5	30- 60	1
12-20	3	60-100	0.6
20-30	2	100-150	0.4
30-40	1.5	150-200	0.3
40-60	1	200-300	0.2

The nominal operating voltage is given by Equation 13.

$$VOP = ITEST \times ZRPOSB + 8 \qquad (13)$$

Where: ITEST is the applied test current
ZRPOSB is the product of the PDT reach set on the front of the DPM10- module, ZT, and the POSB reach multiplier, POSB.
VOP is the nominal operating voltage

The applied voltage should initially be set to a value larger than the nominal operating voltage, and the three phase voltages should be lowered simultaneously until the POSB unit operates, i.e. until pin 22 on the test extender steps from LOW TO HIGH. The actual operating voltage should be within the tolerances given in Table PT-4 for the value of ITEST used.

E. PDX

Use the connections shown in Figure AT-3. Connect temporary jumpers between pins 55, 56, and 60 on a test card extender in the test card position. Connect the oscilloscope input to pin 19 on the test extender.

Set the current and voltage phase angles per Table PT-2. The reach of the PDX unit is equal to the product of the PD1 reach set on the DPM11- module, Z1, and the PDX reach multiplier set on the AEM10- module. The recommended test current is determined by the PDX reach, as shown in Table PT-8. The current used for this test should be equal to or greater than the value given in Table PT-8. The magnitude of all three phase currents should be equal.

TABLE PT-8: PDX Test Current Values

IN=5		IN=1	
ZRPDX	**ITEST**	**ZRPDX**	**ITEST**
1- 6	10	5- 30	2
6-12	5	30- 60	1
12-20	3	60-100	0.6
20-25	2	100-125	0.4

The nominal operating voltage is given by Equation 14.

$$VOP = ITEST \times ZRPDX \qquad (14)$$

Where: ITEST is the applied test current
ZRPDX is the product of the PD1 reach set on the front of the DPM11- module (Z1), and the PDX reach multiplier set on the AEM10- module, (PDX).
VOP is the nominal operating voltage

The applied voltage should initially be set to a value larger than the nominal operating voltage, and the three phase voltages should be lowered simultaneously until the PDX unit operates, i.e. until pin 19 on the test extender steps from LOW TO HIGH. The actual operating voltage should be within the tolerances given in Table PT-4 for the value of ITEST used.

NEGATIVE-SEQUENCE DISTANCE UNITS

A. NDD

Use the test connections shown in Figure AT-4. Connect temporary jumpers between pins 55, 56, 57, 58 and 60 on a test card extender in the test card position. Connect the oscilloscope input to pin 26 on the test extender.

Choose test voltages to be applied to the relay according to the Zone 1 reach as set on the DPM11- module, Z1. Refer to Table PT-9.

TABLE PT-9: NDD Test Voltage/Current

Z1 IN=5	Z1 IN=1	VA	VB	VC	ITEST ∠ -(90+)
1-3	5-15	67∠0	35∠-163	35∠163	$\frac{10.2}{Z1}$
3-12	15-60	67∠0	47∠-135	47∠135	$\frac{33.1}{Z1}$
>12	(>60)	67∠0	58∠-125	58∠125	$\frac{47.3}{Z1}$

Where is the ZR1 angle set on the AEM10- module.

Slowly increase the applied test current until the oscilloscope trace steps from LOW to HIGH. This value of test current should be equal to ITEST, as shown in Table PT-9, with a tolerance given in Table PT-1 for the value of ITEST used.

B. NDD Zone 2 Reach

Use the test connections shown in Figure AT-4. Connect temporary jumpers between pins 55, 56, 57 and 60 on a test card extender in the test card position. Connect the oscilloscope input to pin 26 on the test extender.

The Zone 2 reach of the switched NDD is equal to the Zone 1 reach times the Zone 2 reach multiplier set on the DNM10- module. Choose test voltages to be applied to the relay according to the Zone 2 reach of the ND. Refer to Table PT-9, and substitute the NDDZ2 value for Z1 in the ITEST equation. The NDD Bias is equal to the value set on the DNM10- module multiplied by 67 (to convert from per unit to applied volts).

Slowly increase the applied test current until the oscilloscope trace steps from LOW to HIGH. This value of test current should be equal to ITEST as shown in Table PT-10 with a tolerance given in Table PT-1 for the value of ITEST used.

$$NDDZ2 = Z1 \times Z2 \text{ reach multiplier (on DNM10-)} \qquad (15)$$

C. NDD Zone 3 Reach

Use the test connections shown in Figure AT-4. Connect temporary jumpers between pins 55, 56, 58 and 60 on a test card extender in the test card position. Connect the oscilloscope input to pin 26 on the test extender.

The Zone 3 reach of the switched NDD is equal to the Zone 1 reach times the Zone 3 reach multiplier set on the DNM10- module. Choose test voltages to be applied to the relay according to the Zone 3 reach of the NDD. Refer to Table PT-9, and substitute the NDDZ3 value for Z1 in the ITEST equation. The NDD Bias is equal to the value set on the DNM10- module multiplied by 67 (to convert from per unit to applied volts).

Slowly increase the applied test current until the oscilloscope trace steps from LOW to HIGH. This value of test current should be equal to ITEST as shown in Table PT-9 with a tolerance given in Table PT-1 for the value of ITEST used.

NDDZ3 = Z1 x Z3 reach multiplier (on DNM10-) (16)

D. **ND**

Use the test connections shown in Figure AT-4. Connect temporary jumpers between pins 55, 56, 57, 58 and 60 on a test card extender in the test card position. Connect the oscilloscope input to pin 25 on the test extender.

Choose test voltages to be applied to the relay according to the Zone 1 reach as set on the DPM11- module (PD1 reach). Refer to Table PT-10. The ND Bias is equal to the value set on the DNM10- module multiplied by 67 (to convert from per unit to applied volts).

TABLE PT-10: ND Test Voltage/Current

Z1 IN=5A	Z1 IN=1A	VA	VB	VC	ITEST ∠ -(90+)
1-3	5-15	67∠0	35∠-163	35∠163	$\frac{14+\text{ND BIAS}}{1.16 \times Z1}$
3-12	15-60	67∠0	47∠-135	47∠135	$\frac{42+\text{ND BIAS}}{1.16 \times Z1}$
>12	(>60)	67∠0	58∠-125	58∠125	$\frac{58+\text{ND BIAS}}{1.16 \times Z1}$

Where   is the ZR1 angle set on the AEM10- module.

Slowly increase the applied test current until the oscilloscope trace steps from LOW to HIGH. This value of test current should be equal to ITEST as shown in Table PT-10 with a tolerance given in Table PT-1 for the value of ITEST used.

E. **ND Zone 2 Reach**

Use the test connections shown in Figure AT-4. Connect temporary jumpers between pins 55, 56, 57 and 60 on a test card extender in the test card position. Connect the oscilloscope input to pin 25 on the test extender.

The Zone 2 reach of the switched ND is equal to the Zone 1 reach times the Zone 2 reach multiplier set on the DNM10- module. Choose test voltages to be applied to the relay according to the Zone 2 reach of the ND. Refer to Table PT-10, and substitute the NDZ2 value for Z1 in the ITEST equation. The ND Bias is equal to the value set on the DNM10- module multiplied by 67 (to convert from per unit to applied volts).

Slowly increase the applied test current until the oscilloscope trace steps from LOW to HIGH. This value of test current should be equal to ITEST as shown in Table PT-10 with a tolerance given in Table PT-1 for the value of ITEST used.

NDZ2 = Z1 x Z2 reach multiplier (on DNM 10-) (15)

F. **ND Zone 3 Reach**

Use the test connections shown in Figure AT-4. Connect temporary jumpers between pins 55, 56, 58 and 60 on a test card extender in the test card position. Connect the oscilloscope input to pin 25 on the test extender.

The Zone 3 reach of the switched ND is equal to the Zone 1 reach times the Zone 3 reach multiplier set on the DNM10- module. Choose test voltages to be applied to the relay according to the Zone 3 reach of the ND. Refer to Table PT-10, and substitute the NDZ3 value for Z1 in the ITEST equation. The ND Bias is equal to the value set on the DNM10- module multiplied by 67 (to convert from per unit to applied volts).

Slowly increase the applied test current until the oscilloscope trace steps from LOW to HIGH. This value of test current should be equal to ITEST as shown in Table PT-10 with a tolerance given in Table PT-1 for the value of ITEST used.

NEGATIVE SEQUENCE DIRECTIONAL TESTS

1. **NT** Unit.

Change connections to those shown in Figure AT-5 with relay input Y connected to BH1 or TP9. Move the oscilloscope input to card extender pin No. 23. Set VA = 30 volts RMS, VB = 67 volts RMS, VC = 67 volts RMS. Set angle VB = -120° and angle VC = +120°. Set angle IA = -85°. Slowly increase IA until the oscilloscope trace goes from LOW to HIGH. At this pickup point, current IA should be less than 0.05 (0.01) amperes RMS.

Change angle IA to +95° and check that the oscilloscope trace does not go HIGH as IA is increased up to 10 (2) amperes RMS.

2. **NB** Unit.

Move the oscilloscope input to card extender pin No. 24. Reduce IA to 1.0 (0.2) amperes RMS and check that the oscilloscope trace is HIGH.

Change the angle IA to -85° and check that the oscilloscope trace is LOW.

NDZ3 = Z1 x Z3 reach multiplier (on DNM10-) (16)

PHASE SELECTORS

1. Move the oscilloscope input to card extender pin 27. Set IOP = 1.6 (0.32) amperes RMS and leave all other settings set per step 1 of NEGATIVE-SEQUENCE DIRECTIONAL TESTS. Check that the oscilloscope trace is HIGH.

2. Change connections to those shown for testing PHB SEL in Figure AT-5. Raise VA to 67 volts RMS, lower VB to 30 volts RMS and set angle IOP to -205°. Check that the oscilloscope trace at pin 28 is HIGH.

3. Change connections to those shown for testing PHC SEL in Figure AT-5. Raise VB to 67 volts RMS, lower VC to 30 volts RMS and set angle to -325°. Check that the oscilloscope trace at pin 29 is HIGH.

DIRECTIONAL CHECK

It is often desirable to perform a directional check of the relay system before it is placed in service to insure that the potential and current transformers are phased correctly. This can be accomplished with the PLS relay system using load current and the system voltages. The load current should be greater than 0.5 ampere secondary for this test. If the load current is less, the test may still work if the Fault Detector supervision is defeated by connecting points 55 and 56 on the test card extender to pin 60 (+12 vdc).

For load in the tripping direction, use the XTM test plug connections shown in Fig. PT-1. These connections simulate an internal ϴAG fault by applying rated voltage to phases B and C and zero voltage to phase A while applying current only to phase A. During this test the trip circuits of the PLS should be interrupted to prevent inadvertent tripping of the breaker. Check for a logic one output at pin 23 of the test card extender. This indicates operation of the forward looking directional element, NT. If the load current is in the non - trip direction, use the XTM test plug connections of Fig. PT-2, these connections reverse the ϴA current so that the NT unit will operate for this load flow condition.

XTM TEST PLUGS

Description

The XTM test plugs are designed specifically for post-installation testing of the PLS system. There are two plugs; XTM28L1 (left-hand plug) and XTM28R1 (right-hand plug), each providing access to fourteen relay-side and fourteen system-side points. The system-side points are designated "S" and the relay-side points are designated "R". The plugs are keyed by the contact finger arrangement so that there may be no accidental interchange between the left-hand and right-hand plugs.

The plugs are fitted with a sliding handle that swings out to facilitate wiring to the terminals. The terminals consist of number 8 screws threaded into flat contact plates. The handles each have a tab on the outside edge to guide the wire dress of the test leads.

CAUTION

Not all the external connections to the PLS are wired through the test receptacle.

TERMINAL DESIGNATION

The test receptacle and connection plugs are located to the left of the magnetics module (extreme left-hand position). Their terminals are labeled 1 through 28, with 1 through 14 corresponding to the left-hand side and 15 through 28 corresponding to the right-hand side. These points are designated on the elementary diagram (Figure SD-4) as TP1 through TP28.

The left-hand test plug (XTM28L1) terminals are labeled 1R through 14R and 1S through 14S for the relay side and system side, respectively, with the system side labelled in red. Similarly, the right hand test plug (XTM28R1) terminals are labelled 15R through 28R and 15S through 28S.

XTM TEST CIRCUIT CONNECTIONS

Test circuit connections, designated as TP points in the elementary diagrams, should be made to the relay side of the test plug. Where it is desired to use available system quantities for testing, e.g., DC control power, jumpers may be inserted between the corresponding system side and relay side test plug terminals. Appropriate precautions should be taken when working with station battery DC.

Connections should be made to the test plugs prior to insertion into the PLS.

TEST PLUG INSERTION

To insert the test plugs, the two connection plugs must first be removed. In so doing, electrical continuity is broken between the power system and the PLS for those signals which are wired through the test receptacle (refer to TP points on elementary diagram, Figure SD-4). For the terminals connected to the current transformer secondaries, shorting bars are included on the system side of the test receptacle. These are clearly visible through the transparent plastic face plate on the receptacle. The shorting bars make contact before the connection plug contacts break during removal, so that the CT secondaries are never open-circuited.

Both test plugs may be inserted at the same time. Otherwise, if using only one test plug, the connection plug may remain in the other half of the receptacle.
When the test plugs are inserted into the receptacle, parts of the power system become isolated from the PLS. Refer to the PLS elementary diagram (Figure SD-4) for the TP points associated with each of the test plugs.

WARNING

IT IS CRITICAL THAT JUMPERS BE INSERTED ON THE SYSTEM-SIDE TEST PLUG TERMINALS WHICH ARE CONNECTED TO THE CT SECONDARIES AS SHOWN IN FIGURE SD-4. IF THESE JUMPERS ARE LEFT OUT, THE RESULTING HIGH VOLTAGES DEVELOPED PRESENT A SERIOUS HAZARD TO PERSONNEL AND MAY SEVERELY DAMAGE EQUIPMENT.

CARD EXTENDER

The card extender (GE #0138B7406G1) can be used to examine the input and output levels of each printed circuit module in the relay, as outlined below:

Remove power to the module by turning off the PSM21- module.
Remove the module from the relay.
Insert the card extender into the relay with the connector and test points facing the right hand side of the relay. Make sure the card extender is firmly seated in the relay connector.
Place the module on the card extender, and reapply relay power.
Use extreme caution when probing on modules. Damage to the module or operator may occur if the module or card extender are not handled properly.

The extender has 60 test points which are identified by numbers 1 through 60.

One method of removing power is to turn OFF the power switch on the PSM21- power supply module and then remove both of the connection plugs located in the TPM position on the left side of the case.

Servicing

SERVICING

SPARES

There are two basic approaches that may be followed in servicing the PLS. One approach is field service, where an attempt is made to replace defective components at the relay location. Generally, this will take the most time and require the highest degree of skill and understanding. It can also be expected to result in the longest system-outage time.

The preferred approach is module replacement, where a determination is made as to which function has failed and that function is replaced with a spare module. The system can then be quickly returned to service. Considerable time is saved, and there is much less pressure to make a decision about what to do with the defective part. This approach typically yields the shortest down time. It is recommended that a complete set of spare modules be kept at the main maintenance center.

For those who wish to repair at the component level, drawings are available from the factory. When requesting drawings, the following information must be supplied to the factory:

1. The model number of the module. This is found on the lower part of the front nameplate of each module, e.g. ADM11-.

2. The assembly number of the module. This is found on the component side of the printed circuit board. It is an eight-digit number with a letter inserted between the fourth and fifth digit and suffixed with a group identification, e.g. 0215B5865 G001 or G1.

3. The revision number, this is also found on the printed circuit board, e.g. REV. 1.

WITHOUT THE CONTINUOUS MONITOR MODULE

By inserting an extender card into the test slot, location "B" (see figure MO-1 in the MODULES section), one can gain access to various points throughout the PLS. This feature is extremely useful when testing and servicing the PLS.

If the Continuous Monitor, which is an option that is also a useful device for testing and servicing the PLS, is not provided, a second extender card can be inserted into the slot reserved for it, location "D" (Figure MO-1 in the MODULES section). This gives access to additional points throughout the PLS.

The pin number on the extender card versus signal for the test points (TP-) that are shown in the Logic Diagram, Figure SD-2 (in the SCHEME DESCRIPTION section), is given in Table SE-1. The pin number on the extender card versus the monitor points (CM-), also shown in the Logic Diagram, is given in Table SE-2.

WITH THE CONTINUOUS MONITOR MODULE

When the PLS relay is equipped with the optional Continuous Monitor, many problems can be quickly located. When a failure occurs that causes one or more internal logic levels to shift, this will normally cause one of the many points monitored by the Continuous Monitor to go to an abnormal state. If the monitored point stays in this state for more than 0.5-1 second, the Continuous Monitor will give a Monitor Alarm contact closure. The front panel MON DATA indicator on the TAM101 module, Figure CM-6 in the CONTINUOUS MONITOR section, will also light.

There are two different methods by which the operator can determine which point or points failed. He can place the front panel DATA-SELECT switch in the MON DATA position and step through the display of abnormal points, using the STEP DISPLAY switch. The numbers of the abnormal points need to be recorded at this time.

The other alternative is to interrogate the Continuous Monitor through the serial data link. If monitor data is requested, the video terminal will display all the abnormal point numbers. The operator can leave these numbers on the screen to work from, or they can be copied from the screen and entered in the log.

These abnormal point numbers are the signal input numbers to the Continuous Monitor. Refer to Table SE-2 to find the mnemonic of the PLS signal connected to this input. Table SE-2 also gives the module where the signal originates. Refer to the system Logic Diagram, Figure SD-2in the SCHEME DESCRIPTION section, and locate the abnormal signal levels on this diagram. Locate the earliest abnormal points, that is, the points closest to the AC inputs to the PLS. The problem is normally ahead of this point. Abnormal points that follow the first abnormal point in a signal path probably do not indicate a failure at these points. If there is an earlier, monitored, logic level in the same signal path that is normal, then the problem will usually be between the normal and the abnormal points.

If there is no earlier logic point, then the AC inputs to the PLS that drive the abnormal logic point should be checked. Refer to the Measuring Functions Block Diagram, Figure SE-1 in this section, and locate the abnormal signal levels on this diagram.

The techniques just described locate failures that resulted in monitor alarms from the Continuous Monitor. If a relay failure is suspected of causing a false trip, then the trip data in the Continuous Monitor must be analyzed. Obtain the trip data point numbers using the front panel controls: DATA SELECT, TRIP DATA, STEP DISPLAY and LCD display, or by using the serial data link. See if point 48 went to its abnormal state, HIGH. If not, the trip did not originate in the trip bus connected to the PLS. If point 48 went abnormal, see if point 47 went HIGH (abnormal state). If so, then there was a system disturbance and the trip probably was probably not a false trip. Check the event recorder, if used, and see if a trip condition did exist.

If there was no fault detector signal (point 47 did not go HIGH), then there was an error in the PLS. As in the case where a Monitor alarm light is lit, look for the earliest abnormal point in the signal path. Replace the module where this abnormal point is located. If the failure cannot be localized as occurring between a normal and abnormal monitored point, then it may be necessary to replace all modules between the abnormal point and the AC inputs that supply signals to the abnormal point.

POWER SUPPLY MODULE

Check the following items if the LED found on the front panel of the PSM21- module (Figure MO-13) fails to light when the Power Supply is turned on:

1. The correct DC supply is applied to the PLS.

2. The connection plugs, located on the left side of the MGM module (see Figure MO-1), are properly inserted into the test receptacle.

3. The condition of the fuse located on the PSM21- module, (Figure MO-13).

4. Check for the correct voltages from the Power Supply Module:

The voltages should be within ±5% of nominal. Check each of the following voltages with respect to pins 1, 30, 31 or 60:

Pins 4 or 34	+24 VDC
Pins 2 or 32	+12 VDC
Pins 29 or 59	-12 VDC

The following voltage is checked with respect to pins 25 or 55, and it should also be within ±5% of nominal:

Pins 21 or 51	+24 VDC

Table SE-1: PLS TEST POINT TABLE

PIN NUMBER	SIGNAL (LOGIC) NAME	MODULE
1	GROUND	
2	FD	AEM11-
3	IMA	AEM10-
4	IMB	AEM10-
5	IMC	AEM10-
6	NVA	AEM10-
7	NVB	AEM10-
8	NVC	AEM10-
9	FDP (OR38)	ULM161
10	I0	AEM11-
11	I1S	AEM11-
12	I1T	AEM11-
13	IB	ADM10-
14	IT	ADM10-
15	IDT	DPM11-
16	ITOC	DPM11-
17	PD1	DPM10-
18	PD1D	DPM11-
19	PDX	AEM10-
20	PDT	DPM10-
21	PDB	DPM10-
22	POSB	DPM10-
23	NT	ADM10-
24	NB	ADM10-
25	ND	DNM10-
26	NDD	DNM10-
27	φA SELECTOR	ULM15-
28	φB SELECTOR	ULM15-
29	φC SELECTOR	ULM15-
30	KEY DTT	ULM15-
31	φA TRIP (AND 22)	ULM15-
32	φB TRIP (AND 23)	ULM15-
33	φC TRIP (AND 24)	ULM15-
34	ANY TRIP (OR27A)	ULM171
35	3P TRIP PERM(OR20A)	ULM181
36	TL7	ULM181
37	TRIP PERM (OR16)	ULM19-

Table SE-1: PLS TEST POINT TABLE CONT'D.

PIN NUMBER	SIGNAL (LOGIC) NAME	MODULE
38	POSBR	DPM11-
39	PERM KEYING(OR18)	ULM19-
40	KEY TRANS 1(OR28)	ULM15-
41	KEY TRANS 2(OR29)	ULM15-
42	RCVR (OR12)	ULM15-
43	LOCAL TRIP (OR10)	ULM19-
44	DIRECT TRIP(OR214)	ULM19-
45	CHANNEL TRIP(AND16)	ULM19-
46	BLOCK ZONE (OR37)	ULM19-
47	MOB (TL6)	ULM19-
48	ANY POLE OPEN(OR32)	ULM181
49	LINE PICKUP (OR42)	ULM181
50	WEAK INFEED (TL16)	ULM19-
51	GROUND	ULM161
52	ZONE 2 TIMER (TL2)	ULM19-
53	ZONE 3 (AND6)	ULM19-
54	TOC PU	DPM11-
55	Test1	ULM161
56	Test2	ULM161
57	Test3	ULM161
58	Test4	ULM161
59	Test5	ADM10-
60	+12	PSM21-

Table SE-2: PLS CONTINUOUS MONITOR POINT TABLE

MONITOR POINT	SIGNAL	SOURCE	SOCKET (H) PIN NO.
4	NAND98	ULM161	43
5	PDX	AEM10-	14
6	PDT	DPM10-	44
7	PD1	DPM11-	15
8	PD1D	DPM11-	45
9	ND	DNM103	37
10	NDD	DNM103	7
11	IT	ADM101	36
12	NT	ADM101	6
13	IDT	DPM11-	35
14	ITOC	DPM11-	5
17	PDB	DPM101	38
18	REMOVE φ SEL (OR100)	ULM19-	9
19	POSB	DPM10-	38
20	φA SELECTOR	DSM20-	9
21	φB SELECTOR	DSM20-	10
22	φC SELECTOR	DSM201	40
23	IB	ADM101	11
24	3I0	AEM10-	25
25	TRIP PERM (OR16)	ULM19-	24
26	CHANNEL TRIP (AND16)	ULM19-	54
27	DIRECT TRIP (OR214)	ULM19-	31
28	WEAK INFEED (TL16)	ULM19-	55
29	LINE PICKUP (OR42)	ULM181	26
30	ZONE II TIMER (TL2)	ULM19-	56
31	ZONE III TIMER (TL3)	ULM19-	27
32	RPI (OR12)	ULM15-	57
33	EXTERNAL TRIP (OR19)	ULM181	49
34	BLOCK ZONE (OR37)	ULM19-	19
35	MOB (TL6)	ULM19-	48
36	ANY POLE OPEN (OR32)	ULM181	18
37	KEY1	ULM15-	47
38	KEY2	ULM15-	17
39	φA TRIP (AND21)	ULM15-	46
40	φB TRIP (AND22)	ULM15-	16
41	φC TRIP (AND23)	ULM15-	51
42	PTFF (OR49)	ULM171	21
43	KEY DTT	ULM15-	50
44	LR (OR62)	ULM171	20
45	3P TRIP (OR20A)	ULM181	8
46	IR (OR59)	ULM171	52
47	FDP (OR38)	ULM161	23
48	ANY TRIP (OR27)	ULM171	53

NOTE: Points 1-14 and 17-44 are scanned in the Monitor and TRIP mode.

Points 45-48 are scanned in the TRIP mode only.

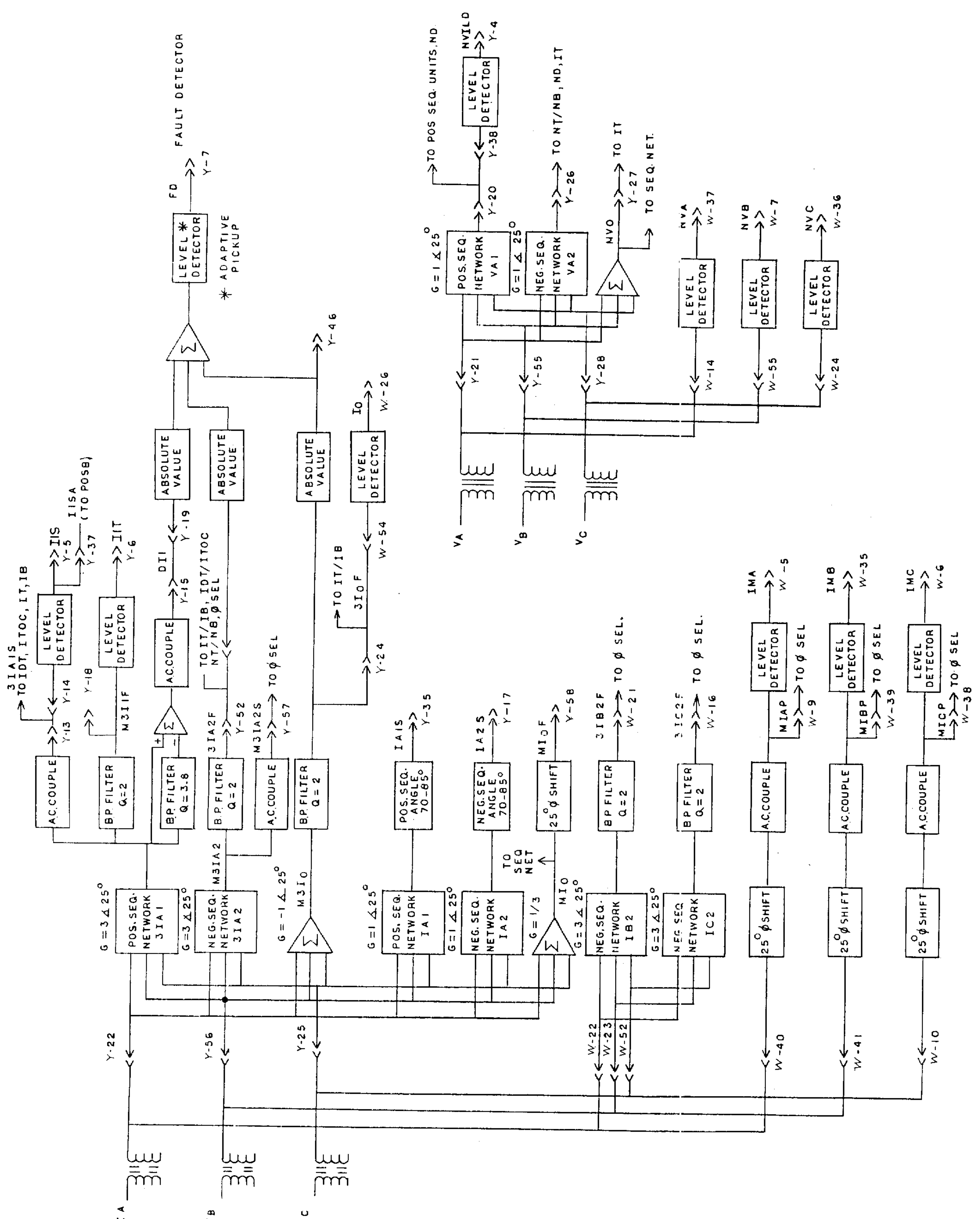


Figure SE-1 (0179C7657 Sh.1[2]) PLS Analog Block Diagram
Current and Voltage Processing

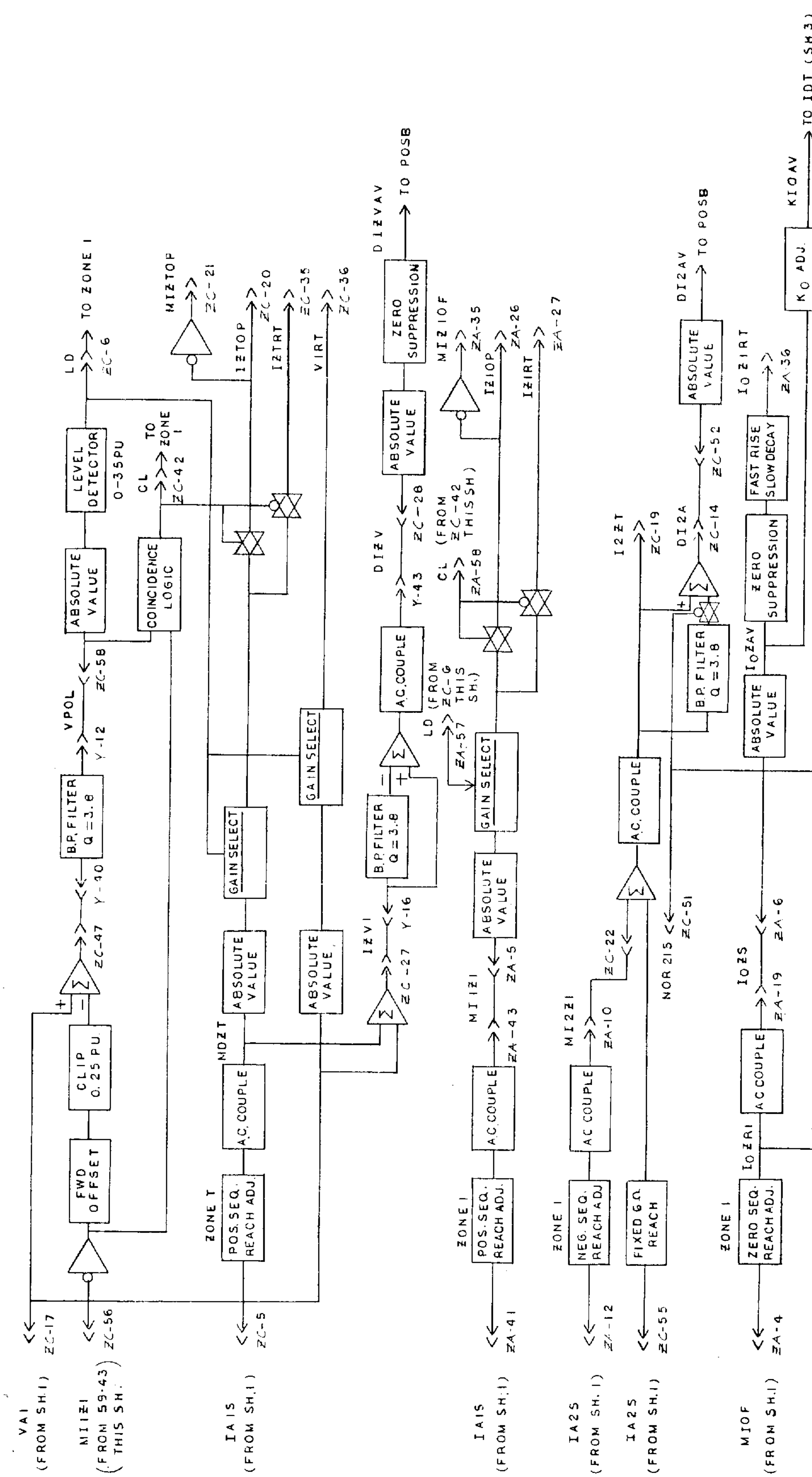


Figure SE-2 (0179C7657 Sh.2[3]) PLS Analog Block Diagram
Reach Adjustment and Polarizing Circuits

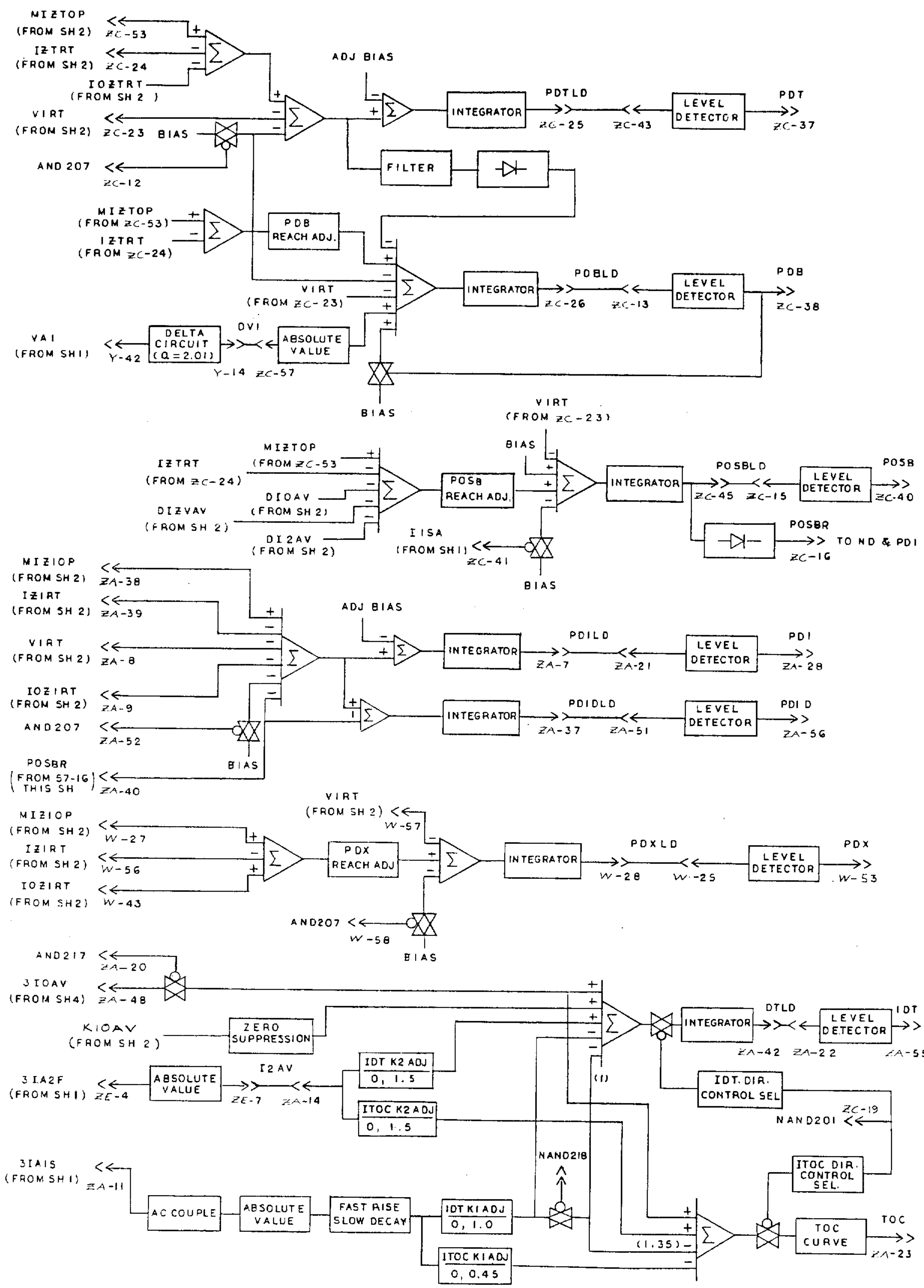


Figure SE-3 (0179C7657 Sh.3[4]) PLS Analog Block Diagram
Positive Sequence Units and IDT, ITOC

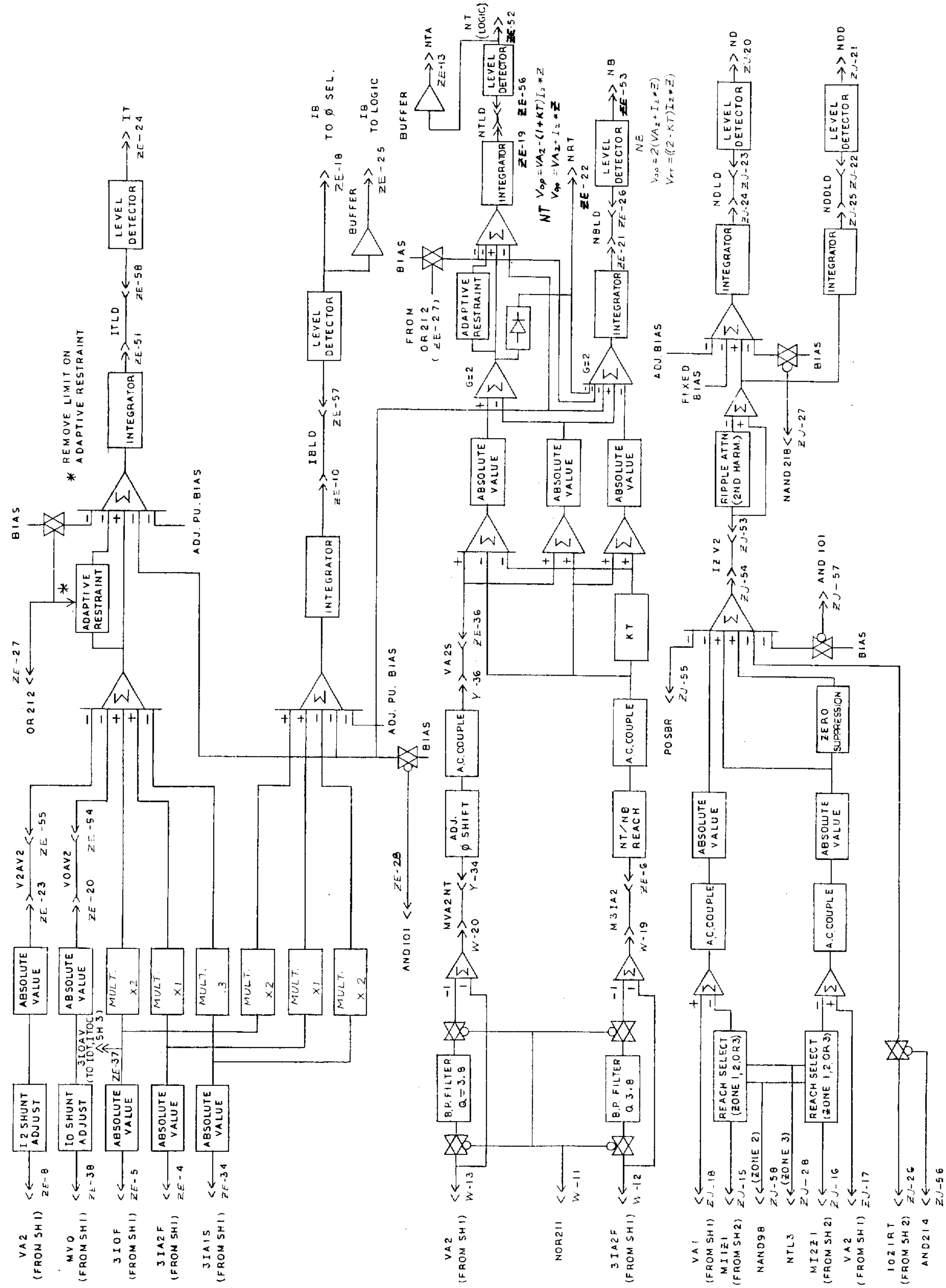


Figure SE-4 (0179C7657Sh.4[3]) PLS Analog Block Diagram
IT, IB, NT, NB, ND, NDD

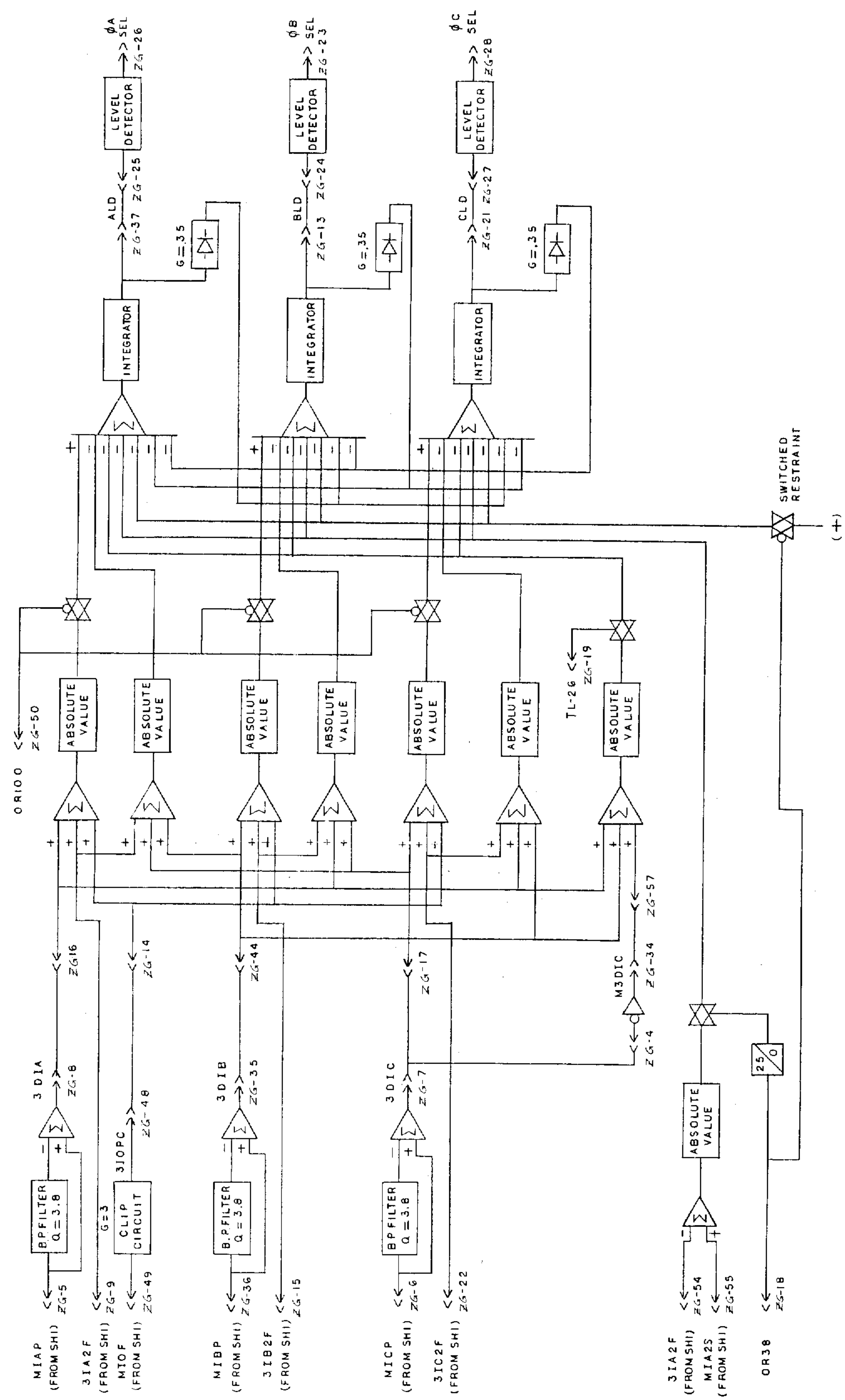


Figure SE-5 (0179C7657 Sh.5[4]) PLS Analog Block Diagram
Phase Selectors

Specifications

SPECIFICATIONS

RATINGS

Rated Frequency	50 or 60 hertz
Rated Voltage	100 to 120 volts AC
Rated Current	I_N = 1 or 5 amperes
DC Control Voltage	48 VDC - Operating Range: 34- 60 VDC 110/125 - Operating Range: 88-150 VDC 220/250 - Operating Range: 176-300 VDC
Maximum Permissible Currents	
Continuous	2 x I_N
Three Seconds	50 x I_N
One Second	100 x I_N
Maximum Permissible AC Voltage	
Continuous	2.0 x rated
One Minute (one per hour)	3.5 x rated
Ambient Temperature Range	
For Storage	-40° to +65° C
For Operation	The PLS has been designed for continuous operation between -20° C and +55° C per ANSI Standard C37.90. In addition, the PLS will not malfunction nor be damaged by operation at temperatures up to +65° C.
Insulation Test Voltage	2 kV 50/60 hertz, one minute
Impulse Voltage Withstand	5 kV peak, 1.2/50 milliseconds, 0.5 joule
Interference Test Withstand	ANSI/IEEE C37.90 and IEC 255-5

BURDENS

Current Circuits	0.03 ohm ∠ 5°, I_N = 5 amps 0.14 ohm ∠30°, I_N = 1 amp	
Voltage Circuits	0.2 VA ∠49°, 60 hertz 0.24 VA ∠48°, 50 hertz	
DC Battery (for contact converters)	1.4 milliamperes each	
DC Battery (for Power Supply and Telephone Relays)	**Normal**	**Tripped**
ALL VOLTAGE RATINGS	15 watts	40 watts

CONTACT DATA

Trip Outputs	Continuous rating = 3 amperes Make and carry for tripping duty: (per ANSI C37.90) 30 amps Break 180 VA resistive at 125/250 VDC Break 60 VA inductive at 125/250 VDC
Auxiliary Outputs (including Alarms)	Continuous rating = 3 amperes Make and carry for 30 seconds: 5 amperes Break 25 watts inductive at 125/250 VDC Make and Carry continuously: 50 watts Maximum of 250 volts or 0.5 amp
DLA and Channel Control Contacts	10 watts 250 VDC maximum 0.5 amp maximum

TABLE SP-1: REACH SETTINGS OF DISTANCE UNITS

			REACH SETTINGS IN OHMS			
			RANGE		RESOLUTION	
FUNCTION	MEASURING UNIT	MODULE	$I_N=5$	$I_N=1$	$I_N=5$	$I_N=1$
ZONE 1	PD1/ND	DPM11-	1 to 25	5 to 125	0.1	0.5
PERMISSIVE ZONE	PDT	DPM10-	2 to 50	10 to 250	0.2	1.0

The reach of the following measuring units is set as multiples of the Zone 1 (PD1) reach or permissive zone (PDT) reach:

Table SP-2: REACH MULTIPLES OF PD1 AND PDT

			REACH IN MULTIPLES OF PD1 or PDT	
FUNCTION	MEASURING UNIT	MODULE	RANGE	RESOLUTION
*ZONE 2 - NEGATIVE SEQ.	N2	DNM10-	1 TO 2.5 X PD1	0.1
*ZONE 3 - NEGATIVE SEQ.	N3	DNM10-	1 TO 4.75 X PD1	0.25
*ZONE 2 - POSITIVE SEQ.	PDX	AEM10-	1 TO 2.5 X PD1	0.1
BLOCKING	PDB	DPM10-	0.5 TO 2.25 X PDT	0.25
OUT OF STEP BLOCKING	POSB	DPM10-	1 TO 2.5 X PDT	0.1

* = Switched Distance Functions

REPLICA IMPEDANCE ANGLE SETTINGS

The replica impedance angle of the distance measuring units is adjustable from 70° to 85° in 5° steps with a board-mounted switch on the AEM11- module.

TABLE SP-3: ADJUSTABLE LOGIC TIMERS

TIMER	MODULE	PU/DO	RANGE	RESOLUTION	DESCRIPTION
TL1	ULM19-	PU	0 - 15.5 ms	0.5 ms	TRIP INTEGRATOR
TL2**	ULM19-	PU	0 - 3.1 sec*	0.1 sec	ZONE TWO
TL3**	ULM19-	PU	0 - 3.1 sec*	0.1 sec	ZONE THREE
TL9	ULM19-	PU	0 - 15 ms	1 ms	REPEAT BLOCK
TL13	ULM15-	PU	0 - 15 ms	1 ms	DTT
TL16**	ULM19-	PU	0 - 75 ms*	5 ms	WEAK INFEED
TL22	ULM15-	PU	0 - 3.1 sec	0.1 sec	DTT RECLOSE BLOCK
TL24	ULM19-	DO	10-120 ms	10 ms	NB DROPOUT
TL25	ULM19-	DO	10-120 ms	10 ms	MB DROPOUT
TL26	ULM171	PU	0 - 77.5 ms	2.5 ms	ANY TRIP BUS

* Can be defeated by setting to OUT
** Located on the front panel

ACCURACY

Distance Measuring Units

Reach: + 5% of setting at angle of maximum reach and rated current

Angle of Maximum Reach: + 3° of setting

Zone Timers

+ 3% of setting

DIMENSIONS

Standard rack-mounted unit:

13-15/16 inches (354 millimeters) high
19-1/16 inches (484 millimeters) wide
(standard 19-inch rack)
14 inches (356 millimeters) deep
(including terminal blocks)

WEIGHT

Standard rack-mounted unit weighs approximately 42 pounds (19 kilograms) net.

Continuous Monitor

CONTINUOUS MONITOR

BASIC OPERATION

The continuous monitor function works on the principle of recognizing a change in state of one or more of up to 40 monitored points (reference Table SE-2 in the SERVICING section) as an abnormal relay system condition if this change in state occurs when the power system is in a quiescent state. This means that the process must know the state of the power system at all times (i.e., quiescent or fault). A fault detector (FD) is used to determine the state of the power system. This same fault detector may also be used to supervise a trip output from the relay system's scheme logic, even if the optional Continuous Monitor module is not included. The fault detector responds to negative-sequence current as well as the change in the positive-sequence current.

A microprocessor, software stored in an EPROM, and other required support chips are the hardware/software that comprise the Continuous Monitor module. The module operation can be described functionally with the aid of Figure CM-1. If one or more of the monitored points changes state (either logic level 0 to 1 or logic level 1 to 0), the fault detector has not operated, and this condition persists for a minimum of 5 seconds, then the Continuous Monitor module issues an alarm output to indicate that an abnormal condition - a relay system failure - has occurred. Based on the actual software and hardware implementation, the "A" time delay in Figure CM-1 is not a fixed value, but rather a statistically variable 5 seconds minimum and 10 seconds maximum. An alarm output is also produced if a fault detector output persists for 60 seconds. This would be an indication that the fault detector itself had failed.

No monitor data will be taken after a bad fault detector is sensed. To alert the user, the program displays "Fd" on the front panel LED numeric display after it senses a bad fault detector. It is still possible to use the STEP DISP. pushbutton to step through the trip and monitor data already stored. If this is done, the "Fd" does not reappear on the display. For this reason, the LED labeled MON. DATA on the front panel is made to blink continuously after a fault-detector failure. This alerts the operator to the fact the unit is not operating normally.

Once OR1 in Figure CM-1 produces an output, indicating a relay system failure, the microprocessor program stores bit patterns in non- volatile memory that identify which monitored point(s) changed state. These "faulty" monitored points are not stored in chronological order, nor time-tagged, but are simply accumulated in memory. Repeated operation and reset of a particular monitored point does not result in this point being stored more than once. This accumulation of "faulty" monitored points continues until the memory is cleared. Since non-volatile memory is used, the data is not lost if the DC power supply is turned off or the DC is removed externally. To clear the memory, a CLEAR command must be given by either (1) the operator pushing a button on the front panel of the module or (2) a remote terminal communicating with the module via a serial data link. When the first relay-system failure is detected, the Continuous Monitor module closes an alarm contact that remains closed until the memory is cleared.

ADDITIONAL FUNCTION

The primary function of the Continuous Monitor module is to detect and to alarm for a relay-system failure. The other function is to store in non-volatile memory those monitored points that have changed state during a relay-system trip output. Following a trip output, the Continuous Monitor module scans the monitored points for 10 milliseconds. Any points that change state within this 10 millisecond interval are accumulated in memory as trip data. This can be useful in analyzing relay-system response to particular faults. This function and its memory are separate and distinct from the primary function of detecting relay-system failures. The Continuous Monitor module can have both "trip data" and "monitor data" in memory at the same time.

Data for five (5) trip events will be stored sequentially. If a sixth trip event occurs prior to the memory being cleared, then the data for the first trip event will be overwritten by the data for the sixth trip event. Thus the data for the five most recent trip events will be retained.

The front panel LED numeric display shows "Fb" when the trip input to the Continuous Monitor is HIGH. This was done to make the unit easier to test. Without this feature, it is difficult to avoid the appearance of Continuous Monitor failure when the trip input is accidentally held HIGH. This makes it difficult to diagnose the real condition.

ACCESS OF STORED DATA

The bottom of Figure CM-5 shows the front panel of the Continuous Monitor module with its LEDs, two-digit LED numeric display, toggle switch and pushbuttons. The stored data, either monitor or trip, can be accessed locally at the front panel of the module, or it can be accessed from a remote terminal via an optional serial data link.

Local Access

For local access, the two LEDs on the front panel of the module indicate that monitor data and/or trip data are stored in memory. A DATA SELECT toggle switch is used to select which data are to be accessed. The step display (STEP DISP.) pushbutton is then pushed repeatedly to cause the stored points to be displayed via the two- digit point number (POINT NO.) LED numeric display.

After the DATA SELECT switch is set to the monitor data (MON DATA) position, the LED numeric display should show 0/0 (i.e., the upper and lower display digits are both zero) to indicate the beginning of the monitor data. If 0/0 is not displayed, the STEP DISP. pushbutton should be pushed to bring the display to 0/0. The next push of the STEP DISP. pushbutton will cause the first stored monitor point to be displayed and this process is continued until 0/0 reappears on the LED numeric display to signal the end of the monitor data.

After the DATA SELECT switch is set to the TRIP DATA position, a 0/0 on the LED numeric display indicates the beginning of the trip data. Once again, successive operations of the STEP DISP. pushbutton cause all the trip data to be displayed between the initial 0/0 and the subsequent 0/0. However, additional codes, E/1, E/2 through E/5 are displayed to differentiate between the trip events. E/1 refers to the last trip event, E/2 to the next-to-last trip event, and E/5 to the earliest stored trip event, assuming five trip events are stored in memory. When starting from 0/0, the first push of the STEP DISP. pushbutton will cause E/1 to appear on the LED numeric display. Successive operations of the STEP DISP. pushbutton will cause all trip data points associated with the last trip event to be displayed, followed by E/2 to indicate the beginning of the trip data points associated with the next-to-last trip event. This continues until 0/0 is displayed to indicate the end of the trip data.

Remote Access

For remote access, a serial data link must be supplied. The Continuous Monitor module includes the necessary software to operate with a serial data link and the chassis backplane wiring connects the input/output ports to a 25-pin connector on the rear of the chassis. This connector resembles an RS-232 connector, but it does **not** provide an RS-232 interface. To provide serial data transmission, an optional, small, fiber-optic transmitter/receiver module (FOM101) can be supplied, which consists of standard Hewlett-Packard devices using SMA connectors and packaged by GE into a connector housing. This device is simply plugged into the 25-pin connector on the rear of the chassis. One means of completing the serial data link is to connect one end of a fiber-optic cable to the small fiber-optic transmitter/receiver module on the rear of the relay chassis and the other end to a commercially available fiber-optic-to-RS-232 converter.

The RS-232 side of the converter can then be connected to a modem to provide remote access via telephone lines, as shown in Figure CM-2. Either a "dumb" or a "smart" terminal may be used at the remote site, since no terminal software is required.

The serial data link option provides the user with the capability of remotely interrogating the Continuous Monitor module to read the data in memory and to clear the memory. Clearing the memory also clears the alarm contact. In the examples below, the full-duplex system as shown in Figure CM-2 is assumed, and the entries by the operator at the terminal are shown in parentheses. Carriage returns are not indicated, but every entry **must** be followed by a carriage return. Entries must be exactly as shown; extra spaces or added punctuation may cause the message to be ignored.

The first step in obtaining data remotely is to address the particular Continuous Monitor module by its identifying number (up to 16 unit-identification numbers can be assigned via an on-board switch setting on the module). This module or unit-number designation allows several modules at one substation to be addressed via one serial data link. Assume that unit 2 is to be addressed. Enter the following at the keyboard:

(***2)

The Continuous Monitor module will respond with one of the following messages:

***2 N	No data in memory
***2 M	Monitor data only in memory
***2 T	Trip data only in memory
***2 M T	Monitor and trip data in memory

Assume that "***2 M T" is received, indicating the presence of both monitor and trip data.

To access the monitor data, enter the following at the keyboard:

(MON)

Assume the response is:

***2 MON
03 09 31

In this case, points 3, 9 and 31 are stored in memory.

To access the trip data, enter the following at the keyboard:

(TRIP)

Assume the response is:

***2 TRIP
06 20 21 22 25 37

06 20 21 22 25 37

The first line of data is for the most recent trip, while the last line is for the earliest trip in memory. In this example data are shown for two trip events, but up to 5 events could be present.

If a different Continuous Monitor module served by the same link is to be accessed at this time, it will be necessary to deselect the present module by issuing a QUIT command, and then to address the next module. To quit a module, enter the following at the keyboard:

(QUIT)

The QUIT command does not erase the memory of the currently addressed module. It does deselect and return to normal mode any unit receiving the command, whether selected or not.

Clearing the Stored Data

The data can be cleared from memory either locally, via the module's front panel, or remotely, via the serial data link. Local clearing is accomplished by pushing the CLEAR DATA button located on the front of the module. The LED numeric display will show C/C until clearing is complete. Remote clearing of the selected unit is accomplished via the serial data link by entering the following command at the keyboard:

(CLEAR)

The CLEAR command, whether issued locally or remotely, clears both monitor and trip data from memory, and it resets the two contacts associated with the monitor alarm. When issued remotely, the CLEAR command also deselects the present module. If there is only one Continuous Monitor on a communications link, then either QUIT or CLEAR can be used as the final command after interrogation.

If there are multiple Continuous Monitor modules, then QUIT should be used, since it will return all the units on the communication line to the normal state. QUIT will not clear the memory, whereas CLEAR will. If the memory is to be cleared in such cases, CLEAR should be sent to each module, then one QUIT command to return all to the normal state. The monitor alarm contacts close when monitor data is stored in memory, and stay closed until a CLEAR command is issued.

MODES OF OPERATION

The Continuous Monitor module can be thought of as having three modes of operation: (1) monitor mode, (2) local-display mode, and (3) serial-data-link-access mode. Note that regardless of which mode the monitor is in, a relay-system trip will interrupt the program and trip data will be stored. The module is then returned to the monitor mode. Normally the module is in the monitor mode with no local- display-mode bits set. In this condition the module's front panel
LED numeric display will show 0/0.

Local-Display Mode

To enter the local-display mode the operator places the DATA SELECT switch at either the MON DATA or the TRIP DATA position and pushes the STEP DISP. pushbutton. If there has been no trip since the last pass through the program, the program looks at the status (local- display mode) word to see if a display bit is set. There are two local-display-mode bits. One indicates that monitor data is to be displayed on the front panel LED numeric display. The other bit signifies that trip data is to be displayed. Only one of the two bits can be on at one time, and the presence of either bit will prevent use of the serial data link. To exit the local-display mode and return to the monitor mode, the operator changes the position of the DATA SELECT switch and pushes the STEP DISP. pushbutton once so that the LED numeric display shows 0/0. Pushing the CLEAR button will also return the module to the monitor mode but will erase the data. After a 5 minute delay, initiated when the local display mode is first entered, the module will automatically revert to the monitor mode. If an operator happens to leave the module in the local display mode, this automates reversion will prevent the loss of all but the first five minutes of data. While in the local-display mode, the module continues its monitoring, as in the monitor mode, except on those program passes when it sees the STEP DISP. pushbutton operated or when a trip has just occurred.

Serial-Data-Link-Access Mode

When in the serial-data-link-access mode the module does not continue the monitoring it performs in the monitor mode; however, it will record the trip data, then leave the serial-data-access mode. While the Continuous Monitor module is sending or receiving data, local access via the module's front panel is also denied.

Assuming that there is only one Continuous Monitor module that can be addressed by the remote terminal, the normal way to terminate this mode and return to the monitor mode is to issue a CLEAR or QUIT command. If neither command is received, after a 5 minute delay, initiated when the serial-data-link-access mode is first entered, the module will automatically revert to the monitor mode, preventing the loss of all but the first five minutes data.

When addressing several Continuous Monitor modules via one serial data link, all the modules will go to the serial-data-link-access mode when a signal is received over the link. In this case, QUIT will not only deselect the presently addressed module, but also act as a "site global" command, since all of the Continuous Monitor modules will return to the monitor mode. CLEAR will deselect the presently addressed module and clear its memory, but it will not cause all the modules to revert to the monitor mode. If the terminal operator forgets to issue a QUIT command, each module will automatically revert to the monitor mode following expiration of its individual 5 minute delay.

CONTINUOUS MONITOR ADJUSTMENTS

The only adjustment on this board is the address-setting switch. The location of this switch and the bit values of the individual switches are shown in Figure CM-5. The setting is the sum of the switch values. The setting can range from 0 to 15. Values from 10 to 15 correspond to addresses from Capital A to Capital F. This address is used to select a particular Continuous Monitor using the serial data link.

The front panel controls are as follows:

Panel Marking	Description
Point Number	Two-digit LED to display abnormal point input number. Top digit is the most significant.
Step Disp.	Pushbutton to step Point Number to next point (in numerical order).
Trip Data	LED that indicates, when lit, that trip data has been stored.
Mon. Data	LED that indicates, when lit, that monitor data has been stored.
Data Select	Two-position switch to select either trip or monitor data on Point Number display.

Clear Data	Recessed pushbutton that clears all memory data when operated.

CONTINUOUS MONITOR SERIAL LINK USE

The continuous monitor serial data link has the following characteristics:

Baud rate	300
Data bits	7
Parity	odd
Stop bits	1

When shipped, the TYS relay system chassis containing the Continuous Monitor is always wired to operate with the serial data link. To provide serial data transmission, a small fiber-optic transmitter/ receiver module can be installed on the 25-pin connector on the rear of the chassis. This connector resembles an RS-232 connector, but it is **not** RS-232 compatible. This fiber-optic transmitter/receiver module (FOM101) is made by GE and contains only the optical transmitter and receiver to couple to and from the fiber- optic cables. The optical transmitter and receiver are standard Hewlett-Packard devices, HFBR1402 and HFBR2402, which use SMA connectors. The other end of the fiber-optic cables (HFBR-3000 or equivalent) can be coupled to any suitable optical devices. Under normal conditions (no transmission) the fiber-optic transmitter at the chassis is OFF. The receiver at the chassis expects a similar "OFF" signal.

The simplest means of using the fiber-optic link is to purchase commercially available fiber-optic-to-RS-232 converters and related communications equipment. Figures CM-3 and CM-4 show two communication schemes that have been implemented.

CHECKSUM

There is a checksum routine that continually checks for EPROM memory errors. If it detects a failure, the front-panel display will reach "C5". The monitor alarm will operate and monitor bit 16 will be set. If this occurs, the Continuous Monitor module should be replaced.

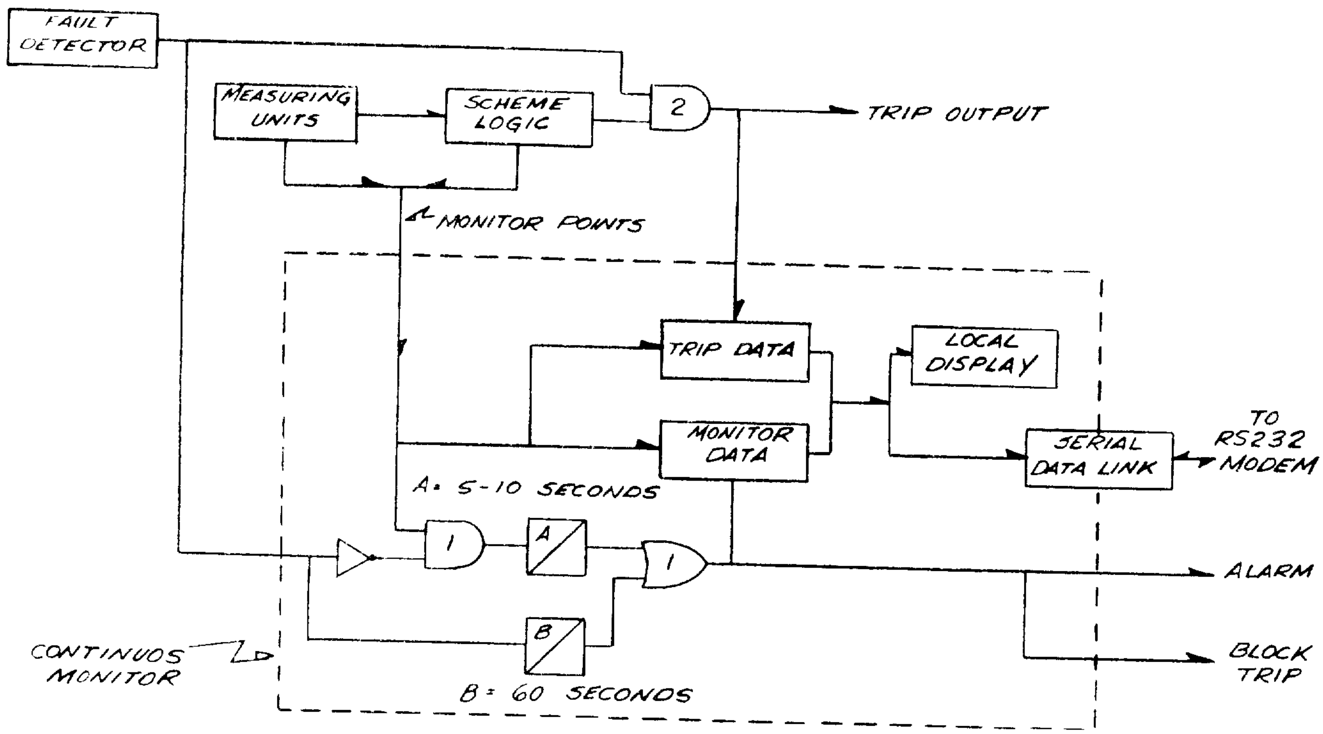


Figure CM-1 (0285A9897) Simplified Functional Diagram Depicting Continuous Monitor Operation

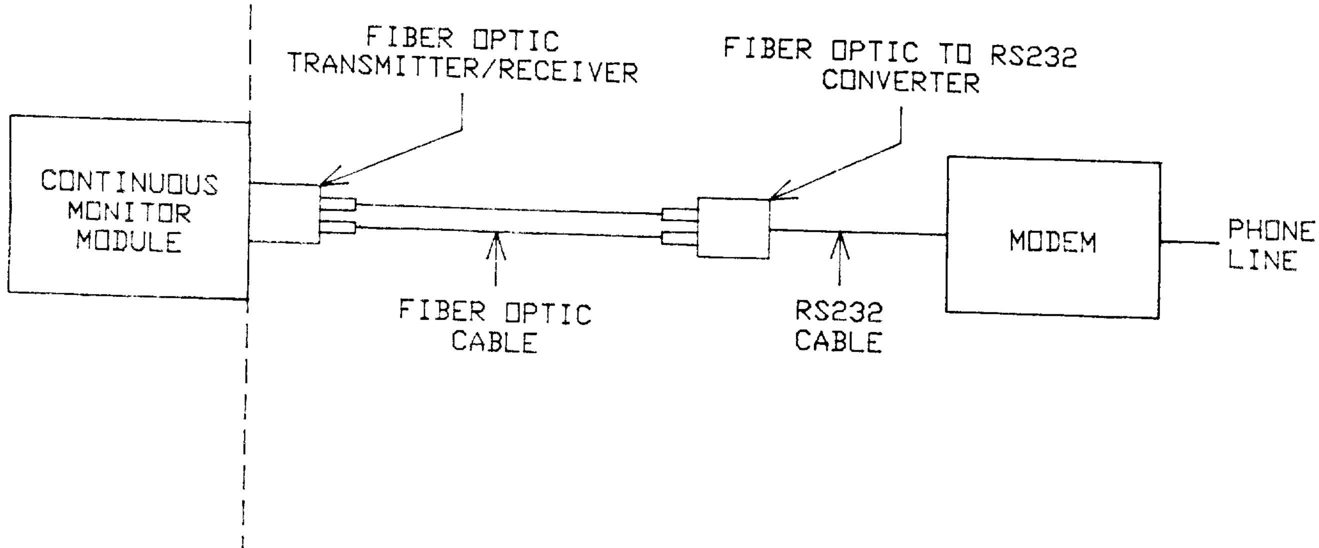


Figure CM-2 (0285A9899 [2]) Serial Data Link Connection

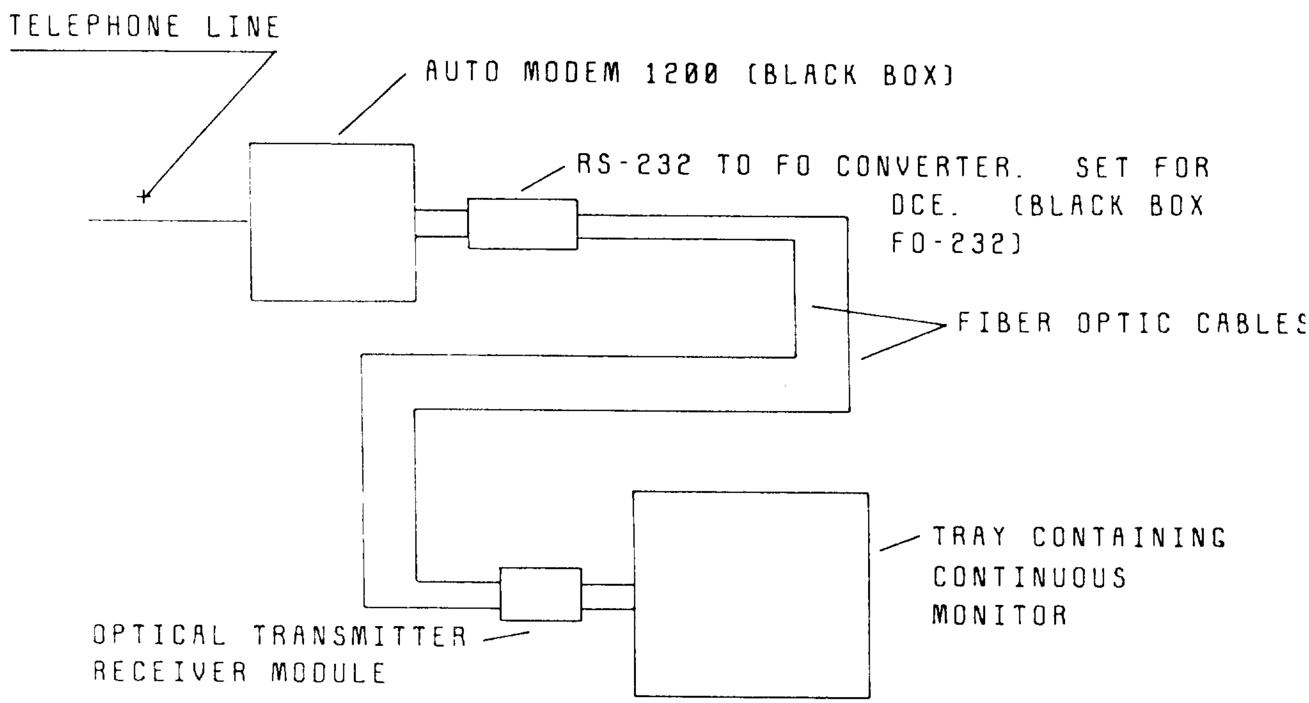


Figure CM-3 (0285A9836 [1]) Continuous Monitor Phone Connection

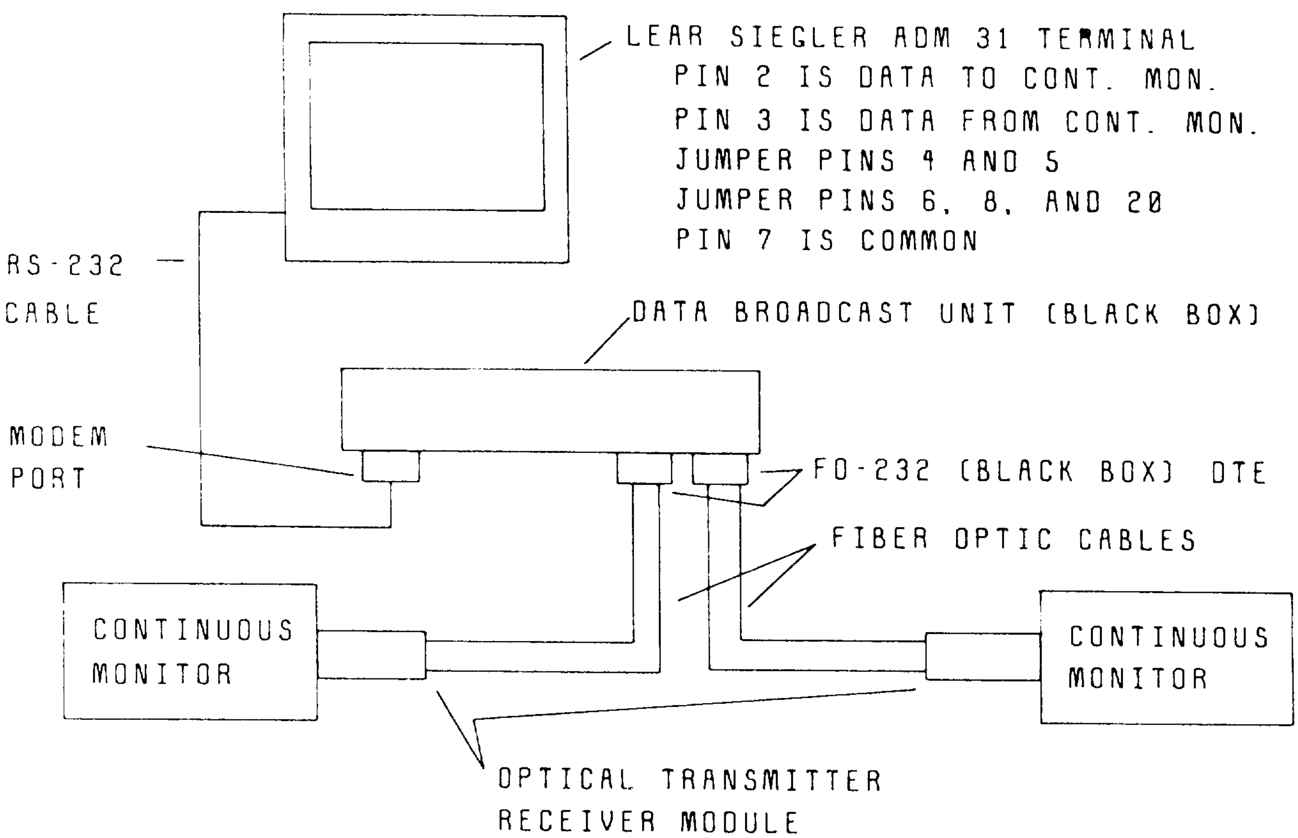


Figure CM-4 (0285A9837 [1]) Connection for Multiple Continuous Monitors

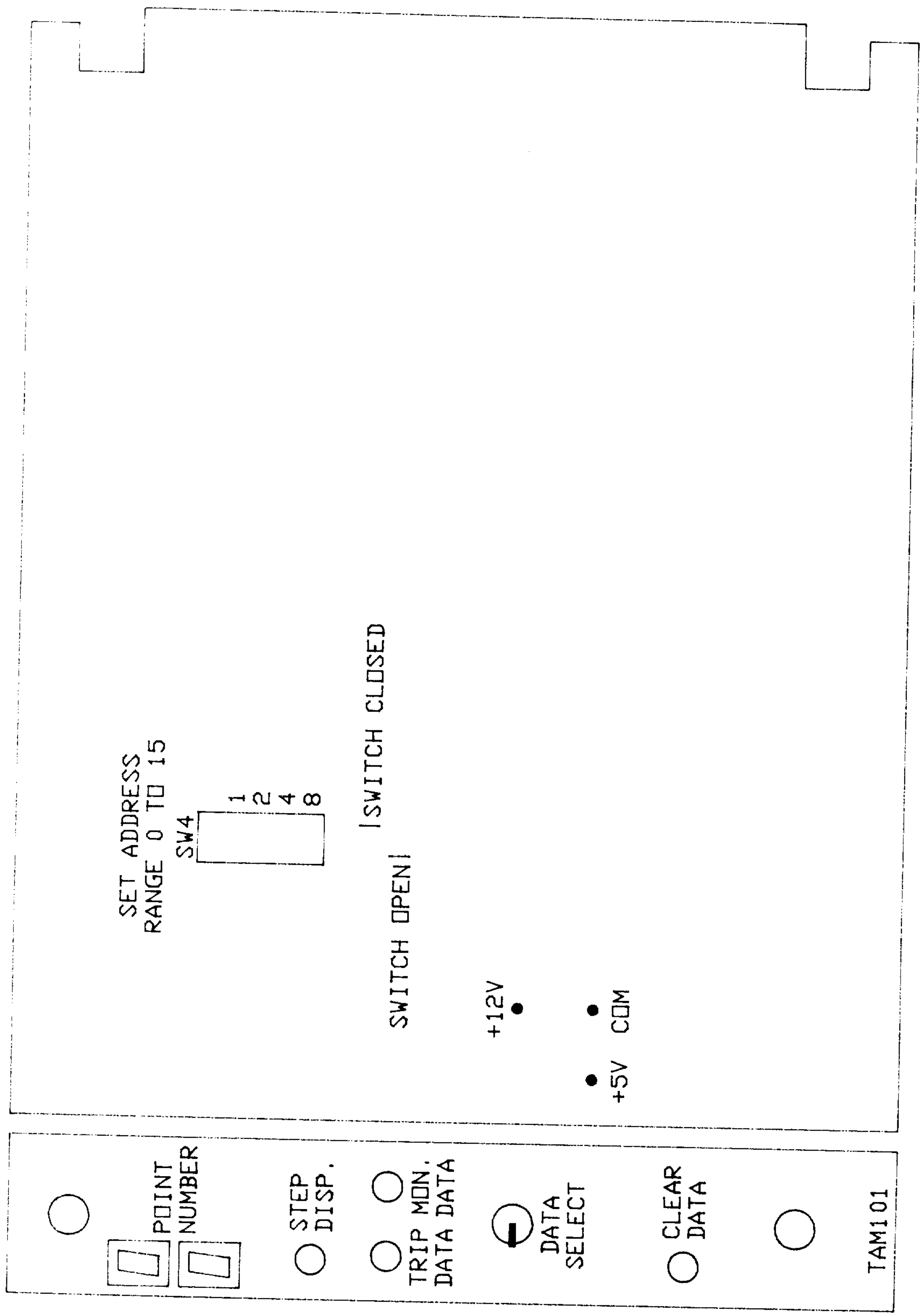


Figure CM-5 (0285A9831 [3]) Front Panel & Internal Switches, TAM101