



**INSTRUCTIONS**

**GEK-45477C**  
Supersedes **GEK-45477B**

**STATIC PHASE SELECTOR**

**TYPE SLS51B**

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**GENERAL  ELECTRIC**

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## STATIC PHASE SELECTOR

### TYPE SLS51B

#### DESCRIPTION

The Type SLS51B relay is used in single pole tripping and reclosing schemes to select the appropriate pole or poles of the breaker(s) to be tripped. The relay has circuits for selecting the faulted phase on single line-to-ground faults, and other circuits for initiating three pole tripping on interphase faults.

The SLS51B relay is packaged in a four rack unit (one rack unit equals 1.75 inches) case. The outline and mounting dimensions are shown in Fig. 2. Component locations are shown in Fig. 3. The internal connections are shown in Fig. 1.

The single pole phase selector circuits provide phase selection for single line-to-ground faults. The phase A selector compares the phase coincidence between  $I_{A2}$  and  $I_{A0}$ .  $I_{A2}$  and  $I_{A0}$  are essentially in phase for A-to-ground faults and 120 degrees out of phase for B-to-ground and C-to-ground faults. Hence the phase relation between  $I_{A2}$  and  $I_{A0}$  provides a reliable method of selecting phase A for A-to-ground faults. Similarly, the phase B selector uses  $I_{B2}$  and  $I_{B0}$ , and the phase C selector uses  $I_{C2}$  and  $I_{C0}$  for phase selection.

The sequence quantities (referred to phase A) are illustrated in Fig. 4 for single line-to-ground faults and double line-to-ground faults. On double line-to-ground faults the single pole phase selectors select the unfaulted phase; that is, for a BC-to-ground fault, the phase A selector operates.

The three pole phase selector circuit consists of two functions, a positive sequence undervoltage function,  $V_1$ , that measures the positive sequence voltage at the relay location; and a compensated positive sequence undervoltage function,  $V_{1X}$ , that is intended to measure the positive sequence voltage at or near the remote end of the line. The compensated positive sequence undervoltage function  $V_{1X}$  has a zero sequence restraint signal to prevent operation on single line-to-ground faults at the near end of the line. The compensated undervoltage function  $V_{1X}$  operates in accordance with the equation

$$\left| V_{IR} - I, Z_R \right| + \left| I_0 Z_R \right| K V_1 \text{ per unit}$$

where:

$V_{IR}$  is the positive sequence voltage at the relay and  $Z_R$  is an adjustable reach setting

$K$  is typically 0.5

*These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.*

*To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.*

## APPLICATION

Reference should be made to the appropriate logic description for application information for the particular application considered.

Typically the single pole phase selectors have a coincidence timer setting of 120 electrical degrees.

The uncompensated undervoltage function  $V_1$  is typically set at one-half the minimum positive sequence voltage that occurs under load (but not fault) conditions on the power system. If line side potential is used, this setting should be checked to ensure it is below the positive sequence voltage occurring when one phase is open on the line after a single pole trip.

The compensated undervoltage function  $V_{1X}$  typically has the same undervoltage setting as the uncompensated undervoltage function  $V_1$ . The positive and zero sequence reach settings ( $Z_R$ ) are typically the same and equal to 125 percent of the positive sequence impedance of the line. However, on series compensated lines a different reach setting may be appropriate depending on the locations of the series capacitors.

## RATINGS

The Type SLS51B relay is designed for use in an environment where the ambient temperature around the relay case is between minus 20°C and plus 65°C.

The Type SLS51B relay requires a plus or minus 15 VDC power source which can be obtained from a Type SSA50/51 power supply.

\* The current circuits of the Type SLS51B relay are rated for five or one amperes, 60 or 50 hertz for continuous duty, and have a one second rating of 250 amperes.

The potential circuits are rated for 120 VAC.

## BURDENS

### DC

The Type SLS51B relay presents a maximum burden to the Type SSA power supply of:

150 ma from the +15 VDC supply

75 ma from the -15 VDC supply

\* AC

	5A, 60 Hz Relay	1A, 50 Hz Relay
Potential Phase-to-Phase	17.1K ohms $\angle 82^\circ$	15.0K ohms $\angle 82^\circ$
Current PL-R Phase $3I_0$	0.04K ohm $\angle 8^\circ$ 0.02K ohm $\angle 30^\circ$	0.74K ohm $\angle 11^\circ$ 0.36K ohm $\angle 10^\circ$

**RANGES**

Each single phase selector has the following sensitivity:

	1A	5A
Ampere negative sequence	0.03	0.15
Ampere $3I_0$	0.06	0.30

The  $V_1$  function has a pickup range of 40 to 80 V RMS.

\* The positive and zero sequence reaches ( $Z$  and  $Z_0$ ) have a range of 5-150 ohms (one ampere) or to 30 ohms (five amperes).

The  $V_{1X}$  function has a pickup range of 40-80 V RMS.

**OPERATING PRINCIPLES**

INTRODUCTION

The SLS51B relay uses signals derived from the secondary currents and voltages as operating quantities for the various measuring functions included in the unit. Signals proportional to positive sequence voltage and current, negative sequence current and zero sequence current are derived in the relay.

POSITIVE SEQUENCE VOLTAGE NETWORK

\* The positive sequence voltage network is shown on the internal connection diagram of Fig. 1. The positive sequence voltage network consists of three phase-to-phase voltage transformers (TA, TB, TC) and an active (using operational amplifiers) sequence network which is contained on the F144 card (50 hertz) or F161 card (60 hertz) in card location H. The voltage at the  $V_1$  test jack is given by the expression:

$$V_1 \text{ test jack} = 0.10 \times V_{1A}$$

where:  $V_{1A}$  is the positive sequence input voltage referenced to phase A.

Potentiometers P1 and P2 are used to cancel small errors due to the potential source which supplies the relay.

POSITIVE SEQUENCE CURRENT NETWORK

The positive sequence current network is shown on the internal connection diagram of Fig. 1. The positive sequence current network consists of three phase-to-phase current transformers (TD, TE, TF), three loading reactors (X1, X2, X3) and an active sequence network on the F143 card (50 hertz) or F160 card (60 hertz) in card location G. The output of the card may be measured at pin 9 of the G card. The voltage at this point is given by the expression:

$$\text{Voltage at pin 9, G card} = 0.22 \times I_{A1} \times \left(\frac{5}{I_N}\right) \angle 0^\circ$$

where:

$I_{A1}$  is the positive sequence component of the input current referenced to phase A

$I_N$  is the rated current (one or five amperes)

NEGATIVE SEQUENCE CURRENT NETWORK

The negative sequence current networks are shown on the internal connections diagram of Fig. 1. The negative sequence current networks use the same current transformers and reactors as the positive sequence current network. Active sequence networks are located on the F170 cards (50 hertz) or F157 cards (60 hertz) in positions D, E and F. The network output may be observed at pin 9 of these cards. Its magnitude is given by:

$$\text{Pin 9 output} = 1.1 \times I_2 \times \left(\frac{5}{I_N}\right)$$

where:

$I_2$  is the magnitude of the negative sequence current in the input current referenced to the associated phase

The outputs of the three cards are 120 degrees out of phase because each network is referenced to a different phase.

ZERO SEQUENCE CURRENT NETWORK

The zero sequence current network is shown on the internal connection diagram of Fig. 1. It consists of a current transformer TG and a loading resistor X4. The input to the CT is the secondary  $3I_0$  current, the output is a voltage proportional to the zero sequence current.

## RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as part of a static relay equipment, mounted in a rack of cabinets with other static relays and test equipment. Immediately upon receipt of a static relay equipment it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust and metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay unit front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

## INSTALLATION TESTS

### CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY.

NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

### CONSTRUCTION

The SLS51B relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The case is suitable for mounting on a standard 19-inch rack. The outline and mounting dimensions and the physical location of the components are shown in Fig. 2 and Fig. 3, respectively. The current and potential quantities enter the SLS51B relay on the twelve-point terminal strips located on the rear of the relay case. The potential connections are made on the RD terminal strip, the current on the RE terminal strip.

The various test jacks are located on the front of the unit. The positive sequence voltage network trimmer potentiometers (P1 and P2) are located on the rear of the unit.

The SLS51B relay also contains printed circuit cards identified by code numbers such as F157, C104, T133, where F designates filter, C designates coincidence, and T designates time delay. The printed circuit cards plug in from the front of the unit. The card sockets are identified by letter designations or "addresses" (D, E, AD, etc.) which appear on the guide strips in front of each socket, on the component location diagram on the internal connection diagram, and on the printed circuit card itself. The tests points (TP1, TP2, etc.) shown on the internal connection diagram, are connected to instrument test jacks on a test card in position T or AT. The jacks are numbered from top to bottom with TP1 to TP10 on the AT card and TP11 to TP20 on the T card. TP1 is connected to relay reference, TP2 is connected to negative (minus) 15 VDC and TP10 to positive (plus) 15 VDC. Output signals are measured with respect to relay reference. Logic signals are approximately plus 15 VDC for the ON or LOGIC ONE condition and less than plus one VDC for the OFF or LOGIC ZERO condition. The output of the filter cards may be analog signals with a range of minus 15 volts to plus 15 volts. The internal connections of the printed circuit cards along with information on design and testing may be found in the printed circuit card instruction book GEK-34158.

Relay signals can be monitored with an oscilloscope, a portable high impedance voltmeter, or the equipment test panel meter. When time-delay cards are to be adjusted or checked, an oscilloscope which can display two traces simultaneously and which has a calibrated horizontal sweep should be used.

\* When the SLS51B relay is supplied mounted in a static relay equipment, the incoming potential and current circuits pass through test receptacles on the equipment test panel. The potential test plug is labeled PTP, the current CTP. These plugs may be replaced with Type XLA test plugs which allow test voltages and currents to be supplied to the relay while maintaining a continuous path for the secondary current.

#### REQUIRED TESTS AND ADJUSTMENTS

The SLS51B is usually supplied from the factory mounted and wired as part of a complete static relay equipment. All units in an equipment are tested together and all unit nameplates carry the equipment summary number. The necessary tests and adjustments are listed below; those marked with a double asterisk must be set by the user. All steps should be performed per the procedures under DETAILED TESTING INSTRUCTIONS to insure that no shipping damage has occurred. The steps should be performed in the order shown.

1. Positive sequence voltage network balance setting\*\*
2. Positive negative sequence current network balance checks
3. Single pole selector checks
4. Three pole selector checks and settings\*\*
  - A. Positive and zero sequence reach setting
  - B. Positive sequence voltage phase shift setting
  - C.  $V_{1X}$  pickup setting
  - D.  $V_1$  pickup setting



DETAILED TESTING INSTRUCTIONS

## 1. Positive Sequence Voltage Balance Setting

The purpose of this test is to adjust the trimmer potentiometers  $P_1$  and  $P_2$ . Because these potentiometers are intended to correct small errors due to unbalance in the potential source, it is necessary to set these potentiometers with the equipment connected to the system. For preliminary tests before installation, these potentiometers may be left at the factory setting.

\* When the SLS51B is mounted in a static relay equipment, the incoming potential circuits pass through the potential test plug (PTP) on the equipment test panel. The plug may be replaced with a Type XLA test plug, and the phase rotation of the source voltage may be reversed on the plug connections. This simulates negative sequence voltage being supplied to the relay. Refer to Fig. 5.

With only negative sequence voltage applied, observe the voltage at the  $V_1$  test jack with an oscilloscope. This voltage should be less than 0.3 volt peak-to-peak and consist primarily of third harmonic. Potentiometers  $P_1$  and  $P_2$  may be alternately adjusted to lower the magnitude of the  $V_1$  test jack.

## 2. Positive/Negative Sequence Current Network Balance Checks

There are no adjustments in the positive or negative sequence current networks. The precision components used for these networks eliminate the need for adjustments. The following procedure will ascertain that the networks are functioning properly.

- \* A) Use the negative sequence connections of Fig. 6. Set the current in each phase to relay rated current (five or one amp). Check for plus or minus 15 volt square waves at the  $I_{A2}$ ,  $I_{B2}$ , and  $I_{C2}$  test jacks. Set the X option plug on the G card to position 4, adjust potentiometer  $P_1$  on the G card fully clockwise; check for less than 1.5 volts peak-to-peak at the  $I_1Z$  test jack.
- \* B) Use the positive sequence connections of Fig. 6. Set the current in each phase to relay rated current. Check for less than ten volts peak-to-peak at the  $I_{A2}$ ,  $I_{B2}$ , and  $I_{C2}$  test jacks. Note that the currents may be adjusted plus or minus 0.10 ampere to achieve this null. A different current adjustment may be needed to achieve the null at each test jack.

Set the X option plug on the G card in position 4, adjust  $P_1$  on the G card fully counterclockwise, set the current for 20 percent of relay rated current per phase. Check that the voltage at the  $I_1Z$  test jack is greater than 7.4 volts RMS.

## 3. Single Pole Phase Selector Checks

## A) Timer DC Pickup and Drop-out Setting

The DC pickup and drop-out of the characteristic timers (T133 cards in positions AE, AG and AJ) can be set using the circuit of Fig. 7. The integrated pickup will be set in Section 4.

Opening the contact causes the output to step to plus 15 VDC after the pickup delay of the timer. Turning potentiometer P<sub>1</sub> (upper pot on card) clockwise increases the pickup delay. Closing the contact causes the output to drop from 15 VDC to less than one VDC after the drop-out delay of the timer.

B) I<sub>0</sub> Phase Shift Setting

The relative phase shift between I<sub>2</sub> and I<sub>0</sub> signals is adjustable by means of the W option plug on the F158 (60 hertz) or F171 (50 hertz) card in card location J. The relative phase shift for each tap setting is shown below:

W OPTION TAP	I <sub>0</sub> LEADS I <sub>2</sub> BY
0	0°
1	10°
2	20°
3	30°

C) Functional Tests

Connect the phase A to ground test circuit of Fig. 8. Set the current for relay rated current. Check that the logic signal at TP14, TP15 and TP16 is at 15 VDC; if it is at reference, remove the appropriate card in the associated Type SLA unit to produce a LOGIC ONE at TP14, TP15 and TP16. Check for continuous output at TP3 (A phase selector) and no output at TP4 and TP5 (B and C phase selectors). Repeat for the B-to-ground and C-to-ground tests of Fig. 8.

4. Three Pole Phase Selector Checks and Settings

A) Positive and Zero Sequence Reach Setting

Connect the phase A to ground test circuit of Fig. 8. Set the current for two times relay rated current. For the positive sequence reach, set the X option plug on the F160 (60 hertz) or F143 (50 hertz) card in position G per the following table. For the zero sequence reach, set the X option plug on the F159 (60 hertz) or F142 (50 hertz) card in position K per the following table.

X OPTION TAP	FIVE AMP RELAY Z <sub>R</sub> OR Z <sub>1</sub> REACH	ONE AMP RELAY Z <sub>R</sub> OR Z <sub>1</sub> REACH
1	12 - 30	60 - 150
2	5 - 12	25 - 60
3	2 - 5	10 - 25
4	1 - 2	5 - 10

NOTE: Use the highest numerical tap possible for the desired setting.

Use potentiometer  $P_1$  on the F159 (60 hertz) or F142 (50 hertz) card in position K to adjust the voltage at the  $I_0Z$  test jack to a value given by the expression:

$$I_0Z \text{ TEST JACK} = 0.675 \times Z_R$$

where:  $Z_R$  is the desired zero sequence reach setting

\*

Use potentiometer  $P_1$  on the F160 (60 hertz) or F143 (50 hertz) card in position G to adjust the voltage at the  $I_1Z$  test jack to a value given by the expression:

$$I_1 \text{ TEST JACK} = 0.675 \times Z_1$$

where:  $Z_1$  is the desired positive sequence reach setting

B) Positive Sequence Voltage Level and Phase Shift Setting

The  $V_1$  phase shift is set by means of the W option plug on the F161 card in position H. The available phase shifts are listed in the following table:

W OPTION TAP	$V_1$ LEADING PHASE SHIFT
0	0°
1	10°
2	20°
3	30°

Connect the positive sequence voltage circuit of Fig. 9. Disconnect all current inputs. Set the voltage for 120 VRMS phase to phase. Check that the voltage at the  $V_1$  test jack is between 6.85 and 7.15 VRMS. If the voltage is outside this range, adjust potentiometer  $P_1$  on the F161 (60 hertz) or F144 (50 hertz) card in position H to obtain 7.0 VRMS at the  $V_1$  test jack.

\*

Set the test voltage for the desired  $V_1$  pickup. Adjust potentiometer  $P_1$  on the D117 card in position AM to just obtain pickup. Note that due to the NOT output of the D117 card, TP7 is at reference when the applied voltage is greater than the pickup setting and at plus 15 VDC when the applied voltage is less than the pickup setting.

Set the test voltage for the desired  $V_{1X}$  pickup. Adjust potentiometer  $P_2$  on the F135 card in position AK to just obtain pickup at TP6. Note that the signal at TP6 is at reference when the applied voltage is greater than the  $V_{1X}$  pickup setting and at plus 15 VDC when the applied voltage is less than the pickup setting.

C) Timer Integration Setting and Three Pole Selector Check

\*

Use the Test I connections of Fig. 10. Adjust the current magnitude to obtain blocks at TP13 which are 4.17 milliseconds (60 hertz) or 5.0 milliseconds (50 hertz) wide. Adjust P<sub>3</sub> on the T133 card in position AL to just obtain output at TP6. Readjust the current to just obtain 6.0 milliseconds (60 hertz) or 7.2 milliseconds (50 hertz) blocks at TP13. Replace the AL timer with a T133 card from position AE, AG or AJ. Adjust P<sub>3</sub> on the card to just obtain pickup at TP6. Return all cards to their original locations.

Use the Test II connections of Fig, 10. Set the phase shifter for an angle of (55° - ∅), where ∅ is the positive sequence voltage phase shift set in Step B.

The value of I<sub>A</sub> test current depends upon the positive sequence reach of the unit (Z<sub>1</sub>). The test current to be used is given in the following table.

\*

X-TAP	1 A RELAY	5 A RELAY	1 A RELAY	5 A RELAY
	Z <sub>1</sub> (OHMS)	Z <sub>1</sub> (OHMS)	I <sub>A</sub> (AMP)	I <sub>A</sub> (AMP)
2,3,4	5 - 60	1 - 12	2	10
1	60 - 150	12 - 30	1	5

Set the applied voltage to a value given by the expression:

$$V = \frac{(I_A Z_1)}{3} (\sqrt{3}) = \frac{I_A Z_1}{\sqrt{3}} \quad (V_{RMS}, \emptyset-\emptyset)$$

The operating point of the V<sub>1X</sub> function (measured at TP6) should be within ten percent of the I<sub>B</sub> test current level given by the expression:

$$I_B = \frac{V_{1X} (\text{pickup}) \sqrt{3}}{Z_0}$$

where: V<sub>1X</sub> (pick up) is the RMS phase-to-phase voltage set previously.

Z<sub>0</sub> is the zero sequence impedance set previously

I<sub>B</sub> is the test current of Fig. 10.

\*

NOTE: Currents greater than two times relay rating should not be continuously applied to the relay.

## PERIODIC CHECKS AND ROUTINE MAINTENANCE

### PERIODIC TESTS

All functions included in the SLS51B relay may be checked at periodic intervals using the procedures described in **INSTALLATION TESTS**. Cable connections between the SLS51B relay and the associated Type SLA logic unit may be checked by observing the test points in the SLA relay.

### TROUBLESHOOTING

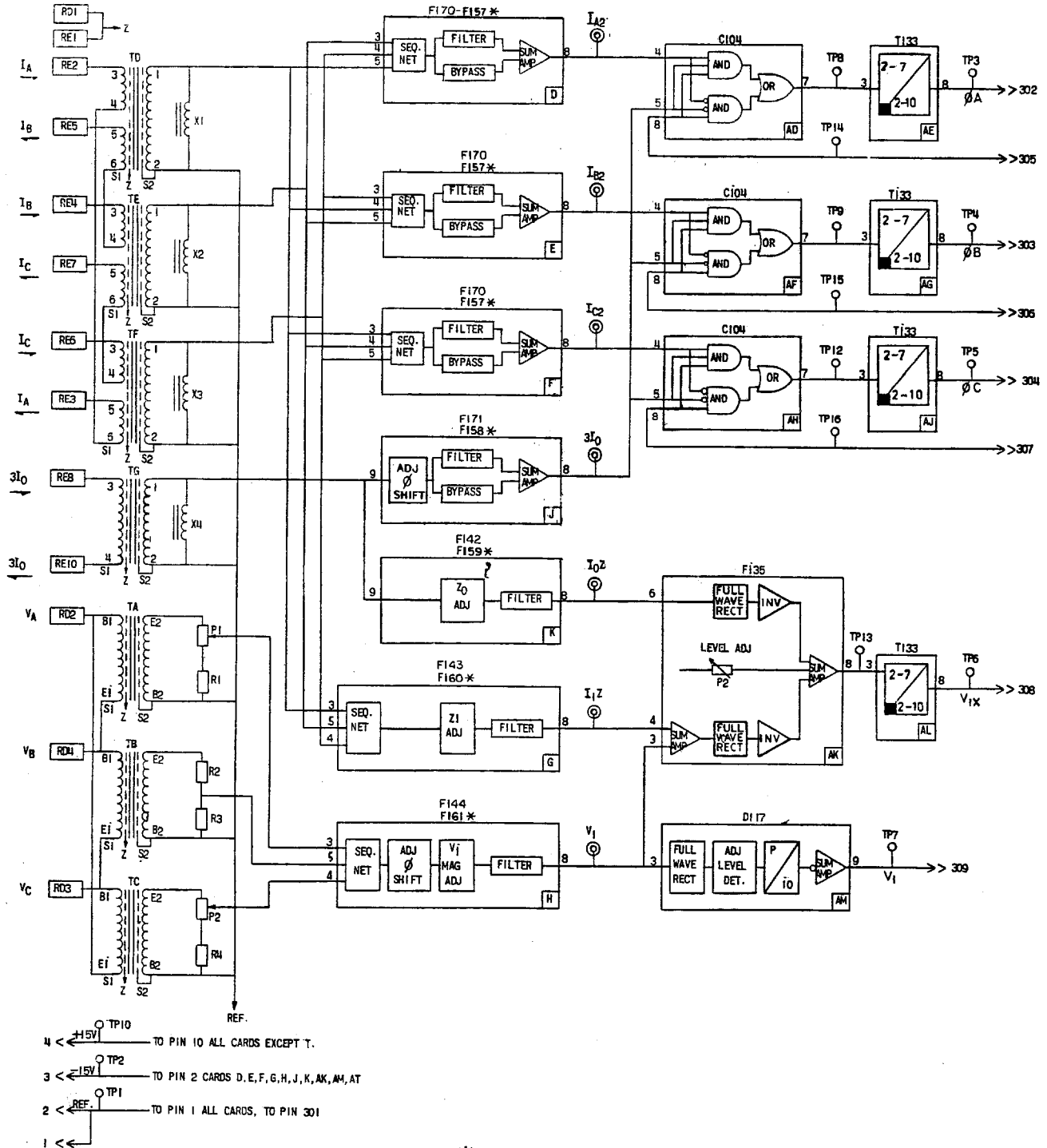
In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

### SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLS51B relay are included in the card book GEK-34158; the card types are shown on the component location diagram, Fig. 3.



COMPONENT VALUES	
R1, R3, R4	500Ω, 5 1/4 W
R2	24Ω, 5 1/4 W
P1, P2	50Ω, 12 1/2 W

* CARD POSITION		D	E	F	G	H	J	K
SLS51B FORM #	1	F157	F157	F157	F160	F161	F158	F159
	2	F157	F157	F157	F160	F161	F158	F159
	3	F170	F170	F170	F143	F144	F171	F142
	4	F170	F170	F170	F143	F144	F171	F142

Fig. 1 (0171C7862-2) Internal Connections Diagram for the Type SLS51B Relay

\*

\*Indicates Revision



RD  
RE

CP12-TOP  
C301-BOT

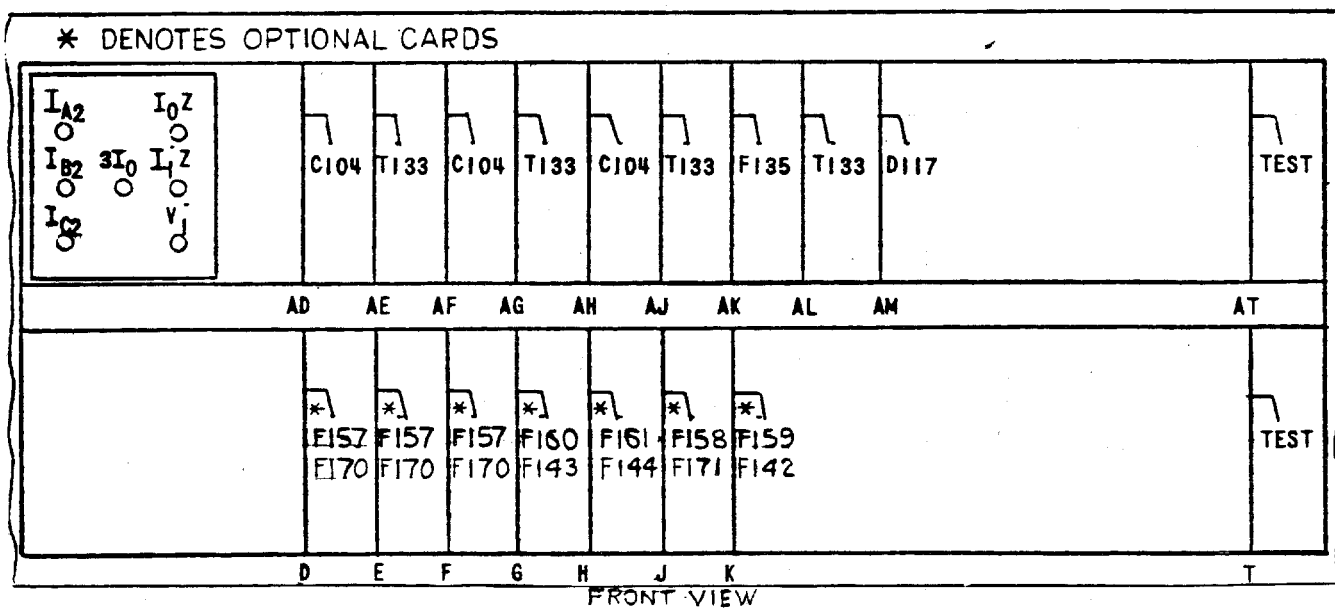
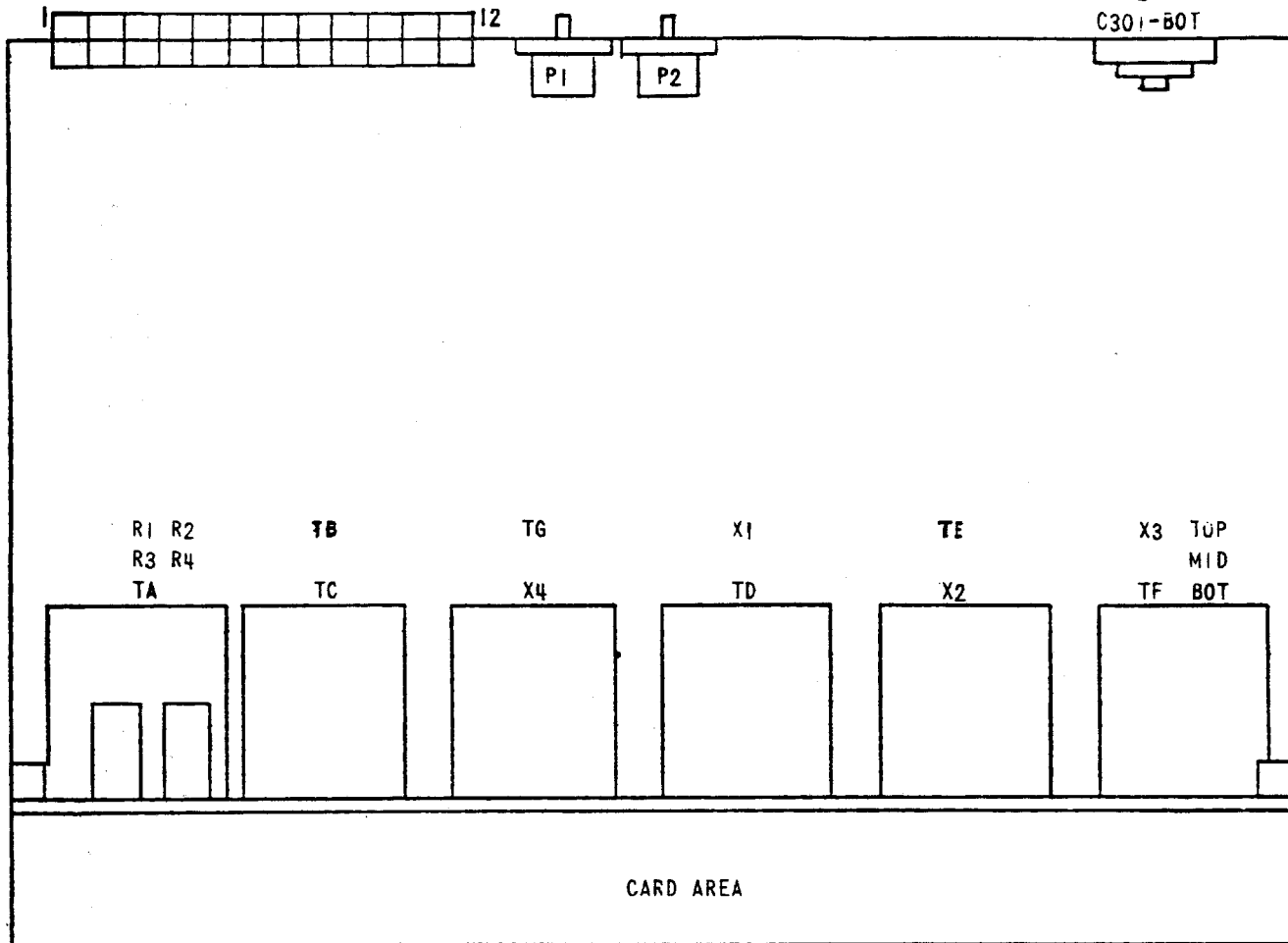
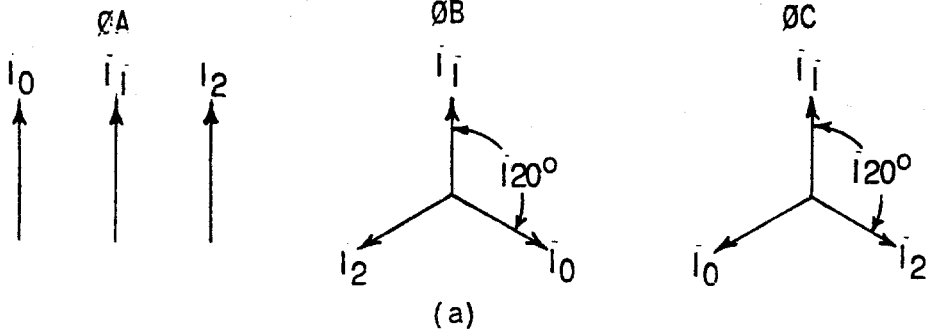


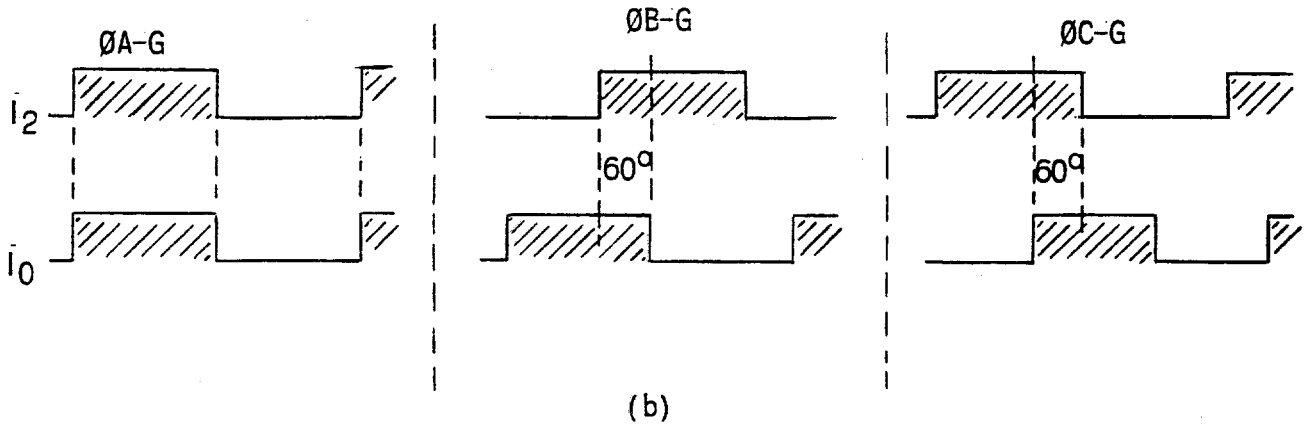
Fig. 3 (0257A8774-1) Component Location Diagram for the Type SLS51B



SEQUENCE QUANTITIES FOR  
SINGLE PHASE-TO-GROUND FAULT



SEQUENCE NETWORK OUTPUTS



SEQUENCE QUANTITIES FOR  
DOUBLE PHASE-TO-GROUND FAULT

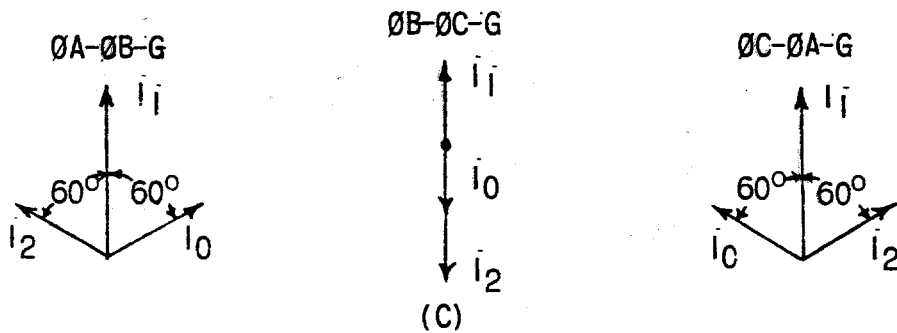


Fig. 4 (0257A6249-1) Sequence Network Inputs and Outputs

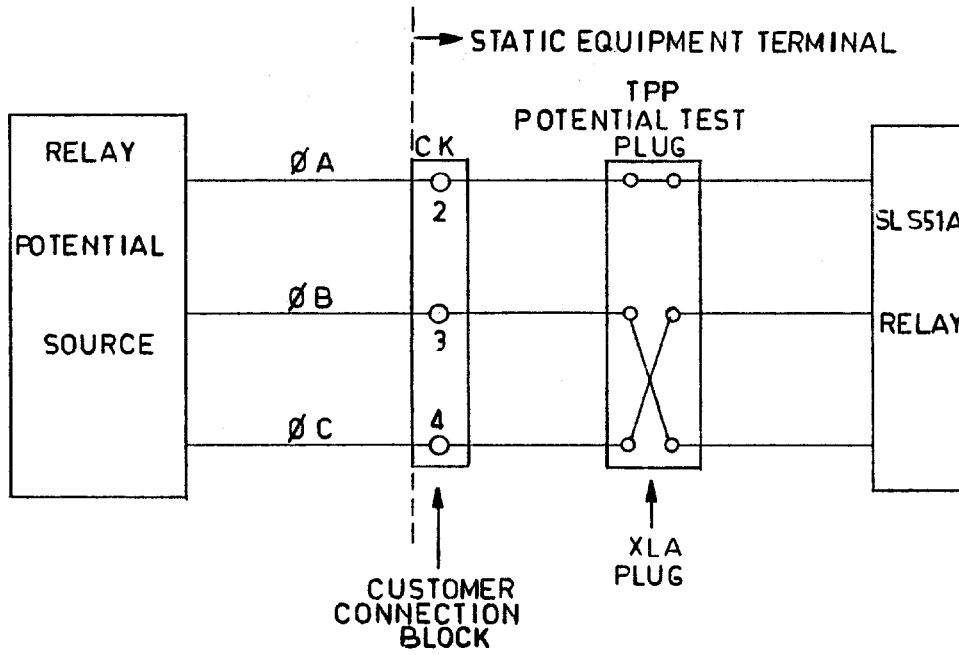


Fig. 5 (0257A8737-0) Connections for Positive Sequence Voltage Network Balance Check

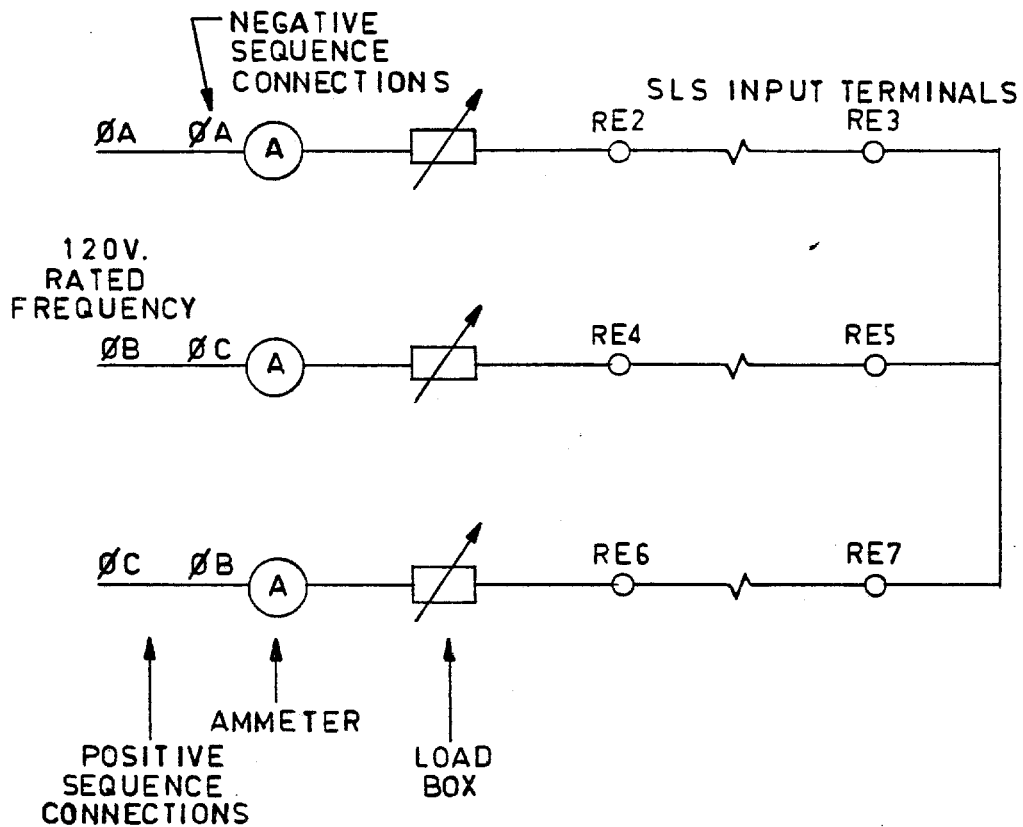
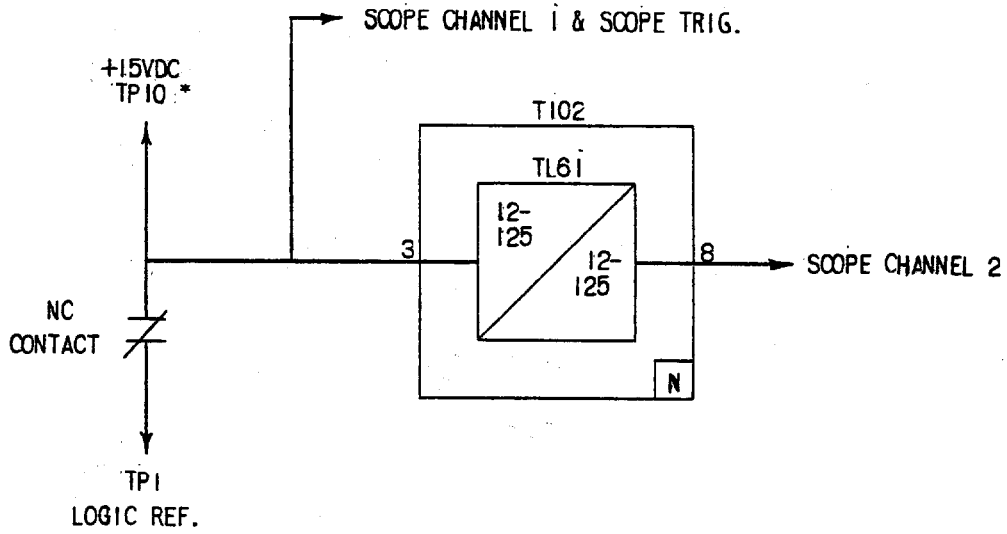


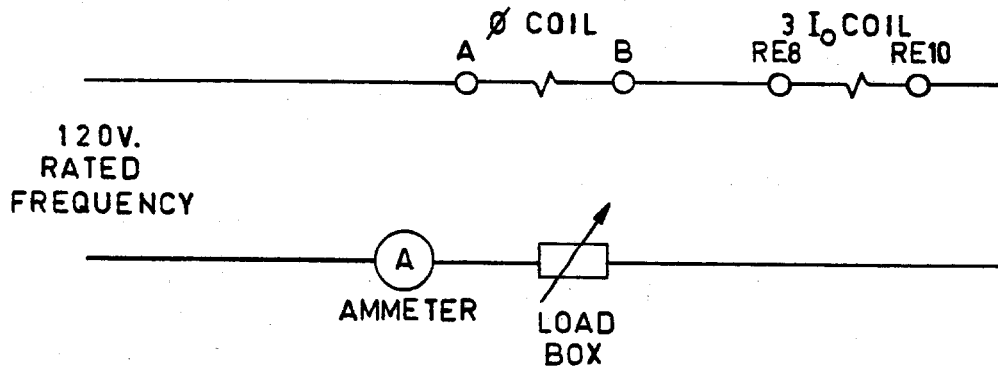
Fig. 6 (0257A8738-0) Connections for Sequence Current Network Balance Check



\* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 7 (0246A7987-0) Timer Test Circuit

SLS 51A INPUT TERMINALS



TEST	A	B
A-G	RE 2	RE 3
B-G	RE 4	RE 5
C-G	RE 6	RE 7

Fig. 8 (0257A8740-0) Connections for Single Pole Phase Selector Checks

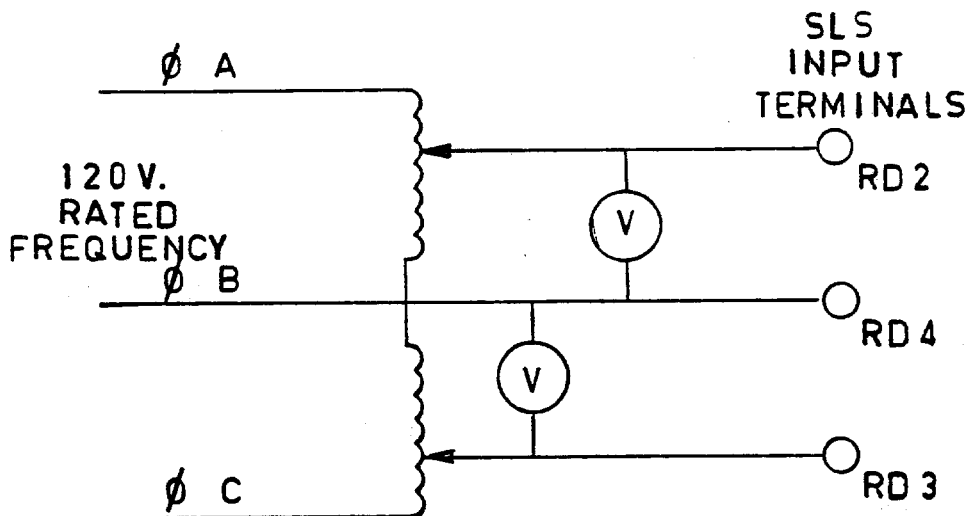
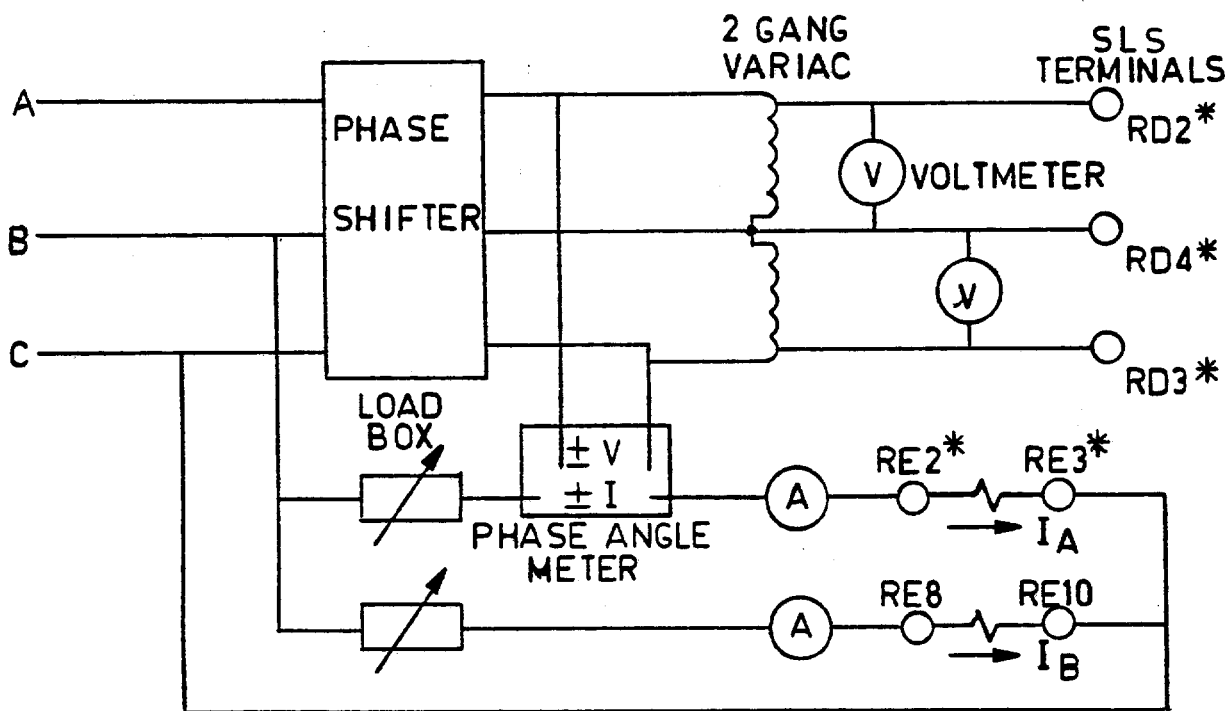


Fig. 9 (0257A8739-1) Connections for Positive Sequence Voltage Level Detector Tests



\* DO NOT MAKE THESE CONNECTIONS FOR TEST I

Fig. 10 (0257A8736-0) Connections for Three Pole Selector Operational Check (TEST II)

