STATIC POSITIVE SEQUENCE DISTANCE RELAY

TYPE SLYP51A
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DESCRIPTION

The SLYP51A is a solid state positive sequence distance relay that is packaged in one 2 rack unit case, the outline and mounting dimensions of which are illustrated in Figure 1.

This relay is not intended for use by itself. Rather it was designed to be employed in conjunction with other solid state measuring and logic relays to provide protection against all types of faults on series compensated lines and on uncompensated lines that are adjacent to series compensated lines. The total complement of functions that may be included in the SLYP51A are noted below.

M1T - Short reach positive sequence directional mho tripping function.
L1T - Long reach positive sequence directional lenz tripping function.
M2B - Offset mho positive sequence blocking function.
MOB - Positive sequence out-of-step detection function. Operates in conjunction with L1T.
V1 - Positive sequence voltage detector.

In general not all of the above functions are included in every SLYP51A since not all are required for all applications. Please refer to the overall logic diagram and the associated description for the specific job involved to determine which functions have been included. This information may also be obtained from the nameplate mounted on the SLYP51A relay since the nameplate lists the ranges of all the included measuring functions.

All SLYP51A relays include the wiring for all the above functions. When any function is omitted in a given relay this function may be added in the field by simply obtaining the necessary printed circuit cards and inserting them in the proper available sockets. However, in order to utilize the function, the proper logic is required in other relays that comprise the total scheme.

The internal connections for the complete SLYP51A are shown in Figure 3 while the component printed circuit card locations are indicated in Figure 2.

APPLICATION

The SLYP51A is a positive sequence relay that is intended to be an integral part of a pilot relaying scheme for use in the protection of series compensated lines or lines adjacent to series compensated lines. It is suitable for use in schemes that employ carrier channels as well as microwave channels.

Of all the above measuring functions in the SLYP51A, the L1T and M2B functions are essential to all schemes. The MOB function is required only if out-of-step detection is to be employed and if no SLLP POSITIVE sequence out-of-step blocking and tripping relay is a part of the scheme.

The V1 function is used for line pick-up protection, loss of potential detection, and certain selective sequential reclosing schemes. It is required only if one or more of these schemes are to be a part of the total scheme of protection.

The M1T function is required only for lines that are longer than 100 miles. In such applications it is used to supplement L1T as part of the pilot scheme.

The basic protective scheme of which the SLYP51A is a part may be routinely applied to all lines up to 200 miles in length where:

a) The source of ac potential to the relays is located on the line side of the series capacitors in the protected line.

b) The compensation in the line does not exceed 80 percent.

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.
c) The series capacitor protective gaps are set to flash at an instantaneous value of voltage that is equal to, or lower than, the peak value of the rated phase-to-neutral voltage of the line.

For the proper external connections for the SLYP51A relay please refer to the elementary diagrams furnished with the overall equipment.

RANGES

The SLYP51A relay has an adjustable system reach of 1 to 30 ohms in the forward (tripping) direction.

The reach of each measuring function in the SLYP51A is fixed at a specific percentage of the relay system reach. For example, if the relay system reach has been set at 4.0 ohms, and the unit nameplate indicates the $M_1T$ reach is 75%, then the reach of the $M_1T$ is $0.75 \times 4 \text{ ohms} = 3$ ohms.

The percentage reach of each function is listed on the SLYP51A unit nameplate. Typical values are shown below:

- $M_1T$ - 75% in the forward direction
- $L_1T$, MOD - 125% in the forward direction
- $M_2B$ - 25% in the forward direction
- 75% in the reverse direction

The SLYP51A relay has an angle of maximum reach which is adjustable between 60 and 90 degrees.

The polarizing quantity of the mho functions may be shifted with respect to the operating quantity. Typical ranges of adjustment are listed below:

- $M_1T$: $-15^\circ$ to $+30^\circ$
- $L_1T$, MOD: $0^\circ$ to $+30^\circ$
- $M_2B$: $-15^\circ$ to $+30^\circ$

The pickup range of the $V_I$ function is seventy to one hundred percent of the rated voltage.

All adjustment ranges for a particular SLYP51A relay are listed on the unit nameplate.

RATINGS

The Type SLYP51A relay is designed for use in an environment where the air temperature outside the relay case is between $-20^\circ\text{C}$ and $+65^\circ\text{C}$.

The Type SLYP51A relay requires a ±15 VDC power source which can be obtained from a Type SSA power supply.

The current circuits of the Type SLYP51A relay are rated at 5 amperes, rated frequency, for continuous duty and have a one second rating of 300 amperes. The potential circuits are rated 120 volts, rated frequency.

CHARACTERISTICS

Operating Principles

The Type SLYP51A relay uses positive sequence voltage and current networks to obtain the $V_I$ and $I_{1Z}$ quantities. These quantities are used to derive the various mho characteristics employed in the SLYP51A relay. The operating theory is described in the following sections.

A. Positive Sequence Voltage Network

The positive sequence voltage network used in the SLYP51A relay is shown in Figure 4. The derivation of the output voltage is described below.

$$V_{out} = V_{B-C} \left( \frac{kP1 + R2}{R1+R2+P1} \right) + V_{C-A} \left( \frac{-mP2}{mP2 + 1/jwc} \right)$$

where K and m are the percents of P1 and P2 used.
By design,
\[
\frac{kP1 + R2}{R1 + R2 + P1} = \frac{1}{2}
\]
and
\[
\frac{m^2P2}{m^2P2 + \frac{1}{3}wc} = \frac{1}{2} \sqrt{60^\circ}
\]
Therefore:
\[
V_{OUT} = \frac{1}{2} V_{B-C} + \frac{1}{2} V_{C-A} \sqrt{60^\circ}
\]
\[
V_A = V_{A0} + V_{A1} + V_{A2}
\]
\[
V_B = V_{A0} + a^2 V_{A1} + a V_{A2}
\]
\[
V_C = V_{A0} + a V_{A1} + a^2 V_{A2}
\]
\[
V_{OUT} = \frac{1}{2} \left[ (V_{A0} + a^2 V_{A1} + a V_{A2}) - (V_{A0} + a V_{A1} + a^2 V_{A2}) \right] + \frac{1}{2} \sqrt{60^\circ} \left[ (V_{A0} + a V_{A1} + a^2 V_{A2}) - (V_{A0} + V_{A1} + V_{A2}) \right]
\]
\[
V_{OUT} = \frac{1}{2} \left[ (a^2 - a) V_{A1} + (a - a^2) V_{A2} \right] + \frac{1}{2} \sqrt{60^\circ} \left[ (a - 1) V_{A1} + (a^2 - 1) V_{A2} \right]
\]
\[
V_{OUT} = .866 \left( V_{A1} \angle -90^\circ + V_{A1} \angle 210^\circ + V_{A2} \angle 90^\circ + V_{A2} \angle 270^\circ \right)
\]
\[
V_{OUT} = 1.5 V_{A1} \angle 240^\circ
\]
For a pure positive sequence input:
\[
V_{OUT} = .866 V_{C-A} \angle 90^\circ
\]

B. Positive Sequence Current Network

The positive sequence current network used in the SLYP5IA relay is shown in Figure 5. The network consists of two transactors (TB and TC), each with two primary windings and an adjustable resistive load across the secondary winding.

The term "transactor" is a contraction of transformer-reactor. It is essentially an air-gap current transformer with secondary current (and therefore secondary voltage across the loading resistor) proportional by its transfer impedance and the associated angle.

\[
Z_T = \frac{V_{OUT}}{I_{IN}} \angle \Theta_T
\]

Where:  
- \(V_{OUT}\) = Secondary output voltage  
- \(I_{IN}\) = Vector sum of the input currents  
- \(\Theta_T\) = Angle by which \(V_{OUT}\) leads \(I_{IN}\)

The derivation of the positive sequence current network output voltage is given below.

By design,
\[
Z_{TC} = .85 \sqrt{3}, Z_{TB}
\]
\[
\Theta_{TB} = 75^\circ
\]
\[
\Theta_{TC} = 45^\circ
\]
\[
V_{OUT} = k \left[ Z_{TB} (I_C - I_B) \angle 75^\circ \right] + Z_{TC} (I_B - 1/3 I_N) \angle 45^\circ
\]
where \(k\) is the percentage of P3 used.
Let \(k = .85\)

5
\[ V_{OUT} = 0.85 \frac{Z_{TB} (I_C - I_B)}{75^\circ} + 0.85 \sqrt{3} \cdot I_B \left( I_B - \frac{1}{3} I_N \right) / 45^\circ \]

\[ V_{OUT} = 0.85 \frac{Z_{TB} \sum \left( I_A0 + a I_A1 + a^2 I_A2 - (I_A0 + a^2 I_A1 + a I_A2) \right)}{75^\circ} + 0.85 \sqrt{3} \cdot Z_{TB} \sum a^2 I_A1 + a I_A2 \] / 45\(^\circ\)

\[ V_{OUT} = 0.85 \sum (a - a^2) I_A1 + (a^2 - a) I_A2] / 75^\circ + 0.85 \sqrt{3} \cdot Z_{TB} \sum a^2 I_A1 + a I_A2 \] / 45\(^\circ\)

\[ = 0.85 \sum (\sqrt{3} \cdot I_A1 / 90^\circ + \sqrt{3} \cdot I_A2 / -90^\circ) / 75^\circ + 0.85 \sqrt{3} \cdot Z_{TB} (I_A1 / 240^\circ + I_A2 / 120^\circ) / 45^\circ \]

\[ = 0.85 \sqrt{3} \cdot Z_{TB} (I_A1 / 165^\circ + I_A1 / 285^\circ + I_A2 / -15^\circ + I_A2 / 165^\circ) \]

\[ = 0.85 \sqrt{3} \cdot Z_{TB} I_A1 / 225^\circ \]

By means of similar manipulations it may be shown that the positive sequence networks of the SLYP51A produce no output when pure negative sequence quantities are applied.

C. Positive Sequence Mho Characteristics

The principle used to derive the mho characteristics is illustrated in Figure 6. The \( I, Z \) quantity is a voltage proportional to the positive sequence current in the line, and is obtained from the positive sequence current filter. The \( V_1 \) quantity is proportional to positive sequence voltage at the relay location and is obtained from the positive sequence voltage network. The quantity \( (I_1Z - V_1) \) is the phasor difference between these two quantities. \( I_1Z' \) is the reverse reach of the relay. The quantity \( (I_1Z' + V_1) \) is the phasor sum of \( I_1Z' \) and \( V_1 \). The angle \( \theta \) between \( (I_1Z - V_1) \) and \( (I_1Z' + V_1) \) is less than 90\(^\circ\) for an impedance point internal to the relay characteristic, equal to 90\(^\circ\) at the balance point, and greater than 90\(^\circ\) for an external impedance point for which the relay should not operate. The quantities \( V_1 \) and \( I_1Z \) are converted into blocks of voltage representing the quantities \( (I_1Z - V_1) \) and \( (I_1Z' + V_1) \). The coincidence of these blocks is then measured. Blocks which are 90\(^\circ\) apart are coincident for 4.17 ms. Blocks which are less than 90\(^\circ\) apart are coincident for more than 4.17 ms. Blocks which are more than 90\(^\circ\) apart are coincident for less than 4.17 ms. The mho function consists of a filter card, a coincidence card, and a timer card which measures the coincidence of \( (I_1Z - V_1) \) and \( (I_1Z' + V_1) \). This circuit is shown in Figure 3.

L1T Function

The resistor \( R_B \), which is mounted on the N101 card in position E, determines the relationship between the reach of the L1T function and the reach of the relay unit. The L1T reach, at the relay angle of maximum reach, may be calculated from the expression:

\[ Z_{MAX} = \frac{K_{TB} \times 100}{T} \]

where:

\( T = \) Voltage restraint tap setting expressed in percent
\( T_B = \) Basic minimum ohmic tap setting
\( R_B = 20K \) \( R_B + 10K \) = percentage reach of L1T/100

The F106 filter card (position G) is supplied with three inputs: \( I_1Z, + V_1, - V_1 \). The outputs of the filter card are 30 VDC square waves (-15 VDC to +15 VDC). The square wave output at pin 9 is the polarizing quantity derived from the +\( V_1 \) input, and the square wave output at pin 8 is the operating quantity derived from -\( (I_1Z - V_1) \). In addition to filtering, the F106 card provides an adjustment of the phase relationship between the output quantities by shifting the polarizing quantity relative to the operating quantity. When the polarizing quantity is shifted, the filter card outputs are -\( (I_1Z - V_1) \) and \( V_{PDL} \) where \( V_1 \) is the positive sequence voltage at the fault and \( V_{PDL} \) is the phase shifter polarizing quantity. L1T operation occurs when the coincidence between \( I_1Z - V_1 \) and \( V_{PDL} \) is equal to the characteristic timer setting.
The construction of the mho characteristic for leading and lagging polarizing voltage is shown in Figure 16. The reach at the relay angle is a chord of all the characteristics. The polarizing phase shift angle ($\rho$) is positive in the counter clockwise direction. The angles $\alpha_1$ and $\alpha_2$ are determined by the characteristic timer setting (TS) and the polarizing phase shift $\rho$:

\[
\begin{align*}
\alpha_1 &= TS - \rho \\
\alpha_2 &= TS + \rho
\end{align*}
\]

The C101 coincidence measurement card (position B) compares the positive half cycle of one square wave with the negative half cycle of the other; when both are present simultaneously an output is produced. The output blocks are thereby produced when $V_1$ and $(i_2 - V_1)$ are coincident. Typical waveforms are shown in Figure 7.

The output blocks from the C101 card are the inputs to the timer card in position N. The timer card produces an output when the width of the input blocks exceeds the pickup setting of the timer. At a given angle (other than the relay angle) the pickup point changes when the pickup setting of the characteristic timer is changed. Increasing the pickup time decreases the fault voltage required for operation.

The other mho characteristics operate in a similar manner.

Operating Characteristics

The operate and reset times of each mho function is basically determined by the characteristic timer, the type of fault and the incidence angle. There is no significant time delay in the circuitry ahead of the timer.

A phase current of one ampere on a three phase fault will cause the SLYP51A relay to pull back to no less than 90% of the nominal reach, with a basic ohmic tap setting (Ib) of 3A.

DC Burden

The Type SLYP51A relay presents a burden to the Type SSA power supply of:

- 200 ma from the +15 VDC supply
- 100 ma from the -15VDC supply

AC Burden

Potential circuits at 120 V $\rho - \rho$

<table>
<thead>
<tr>
<th>PHASE A</th>
<th>PHASE B</th>
<th>PHASE C</th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>0%</td>
<td>100%</td>
</tr>
<tr>
<td>RESTRAINT</td>
<td>7.0</td>
<td>11.5</td>
</tr>
<tr>
<td>VOLT-AMP</td>
<td></td>
<td>5.5</td>
</tr>
<tr>
<td>WATTS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VARS</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Current circuits at 5A $\rho-N$

<table>
<thead>
<tr>
<th>PHASE A</th>
<th>PHASE B</th>
<th>PHASE C</th>
</tr>
</thead>
<tbody>
<tr>
<td>BASE TAP</td>
<td>3RL</td>
<td>3RL</td>
</tr>
<tr>
<td>R</td>
<td>0.0</td>
<td>0.013</td>
</tr>
<tr>
<td>X</td>
<td>0.0</td>
<td>0.013</td>
</tr>
<tr>
<td>Z</td>
<td>0.0</td>
<td>0.018</td>
</tr>
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CALCULATION OF SETTINGS

The proper settings for the measuring functions in the SLYP51A relay will depend to a large degree on the specific application. For this reason, it is recommended that the application information supplied with the description of the overall logic diagram of the total scheme be consulted for the proper considerations and settings. There are a number of adjustments available in this relay but only some of
them are intended for field settings. They are itemized below.

The reach settings of the $L_1T$, $M_1B$, $MOB$ (when used) and $M_1T$ (when used) functions are all made by one common adjustment. This is done in two parts.

With this common setting, the relative reaches of all these functions are fixed at the factory for the specific application of long line (100-200 miles) or short line (less than 100 miles). If for any reason the intended application changes from long to short line or vice versa, it may be necessary to alter the relationship between the reach settings of these units. This may be simply accomplished in the field but the local General Electric Company Sales Office should be consulted for suggested settings.

Since the shape of the $MOB$ characteristic will depend on the application and system conditions, the characteristic timer for this function will require field setting when it is used.

The pick-up voltage setting of the $V_1$ function must be made in the field.

Please refer to the INSTALLATION TESTS section of this instruction book for information on how to make the desired settings on this relay.

**RECEIVING, HANDLING AND STORAGE**

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, and metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately 8 inches back from the relay unit front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

**INSTALLATION TESTS**

**CAUTION**

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTANTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

The Type SLYP51A relay is usually supplied from the factory mounted and wired in a static relay equipment. The following checks and adjustments should be made by the user in accordance with the procedure given under DETAILED TESTING INSTRUCTIONS before the relays are put into service.

1. Positive sequence voltage network balance check*
2. Positive sequence current network balance check*
3. Relay angle of maximum reach setting
4. $L_1Z$ magnitude setting*
5. Voltage restraint tap setting
6. Basic minimum ohmic tap setting
7. $M_1$ characteristic timer setting*
8. $M_1$ characteristic phase angle adjustment
9. Level detector pickup setting

* Factory Setting
Construction

The SLYP51A relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The case is suitable for mounting on a standard 19 inch rack. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 2 respectively.

The tap blocks for making the voltage restraint settings are located on the front panel of the unit. The method of making restraint tap settings is illustrated in Figure 8. The connections are made by means of taper pin connectors; special tools are supplied with each equipment for the removal and insertion of these pin connectors.

The current and potential enter the SLYP51A on twelve point terminal strips located on the rear of the relay case. The potential connections are made on the YA terminal strip, the current connections on the YB terminal strip.

The basic minimum ohmic tap (Tb) setting is accomplished on the YB terminal strip on the rear panel of the unit. The current connections for the 1\(\pi\) and 3\(\pi\) taps are shown in Table I.

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<tr>
<td>1(\pi) BASE REACH</td>
</tr>
<tr>
<td>3(\pi) BASE REACH</td>
</tr>
</tbody>
</table>

The V₁ and I₁Z test jacks, the IZ magnitude reach pot (P6) are located on the front of the unit below and voltage restraint taps. The positive sequence filter potentiometers (P1, P2, P3, P4) are located inside the relay case as shown in Figure 2.

The SLYP51A relay also contains printed circuit cards identified by a code number such as F106, C101, D101, T101, N101, where F designates filter, C designates coincidence, D designates level detector, T designates time delay, and N designates network. The printed circuit cards plug in from the front of the unit. The sockets are identified by letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location diagram, on the internal connection diagram, and on the printed circuit card itself. The test points (TP1, TP2, etc.) shown on the internal connection diagram, are connected to instrument jacks on a test card position T with TP1 at the top of the card. The internal connections of the printed circuit cards are shown in the Printed Circuit Card Instruction Book GEK-34158.

Pin number 1 on the test card in position T is connected to relay reference, number 2 to -15 VDC, and pin number 10 to +15 VDC. Output signals are measured with respect to the reference bus on the test card (TP1). Logic signals are approximately +15 VDC for the ON or LOGIC ONE condition, and less than 1 VDC for the OFF or LOGIC ZERO condition. Filter card outputs are either +15 VDC or -15 VDC for the ON condition.

These outputs can be monitored with an oscilloscope, a portable high impedance DC voltmeter, or the test panel voltmeter if available. When the test panel meter is supplied, it will normally be connected to the reference bus. Placing the relay test lead in the proper test point pin jack will connect the meter for testing. When time delay cards are to be adjusted or checked, an oscilloscope which can display two traces simultaneously and which has a calibrated horizontal sweep should be used.

Detailed Testing Instructions

Before proceeding with the following test program, be sure that the tripping circuits from the associated Type SLAT relay are open.

A. Positive Sequence Network Balance Checks

The voltage and current sequence networks have been accurately preset at the factory to obtain negative sequence cancellation. No further adjustments should be required in the field. It is recommended,
however, that the networks be checked at the time of installation to insure that nothing has occurred during shipment to unbalance the networks.

Positive Sequence Voltage Network

To check the null of the sequence voltage network, use the test circuit of Figure 9 and the connections of Table II. Three three phase-phase voltages should be exactly equal in magnitude and 120° apart. For best resolution, use a voltage near the rated value. If the source voltages are not balanced (within a few percent) a single phase variac should be used to correct the unbalanced phase.

| TABLE II |
|-------------------|---|---|---|
| TEST FIGURE POINT | A | B | C |
| SLYP51A TERMINAL  | YA2 | YA4 | YA3 |

The voltage at the V3 test jack should consist solely of harmonics with no fundamental present. The peak to peak value of the network output will depend on the system, but should be on the order of a few tenths of a volt.

If the network needs readjustment to eliminate the 60 Hz fundamental, set P1 and P2 at midrange. Alternately make small adjustments in P1 and P2 until the desired level is achieved.

Positive Sequence Current Network

Method I - Three Phase Test Source

To check the null of the sequence current network, use the test circuit of Figure 10 and the connections of Table III. The three currents should be exactly equal in magnitude and 120° apart. Rated current (5A) will provide best resolution. If the source voltages are not balanced (within a few percent) a single phase variac should be used to correct the unbalanced phase.

| TABLE III |
|-------------------|---|---|---|
| TEST FIGURE POINT | D | E | F | G |
| SLYP51A TERMINAL  | YB7 | YB5 | YB3 | YB1 |

Jumper H to I

The voltage at the I3Z test jack should consist solely of harmonics with no fundamental present. The peak to peak value of the network output will depend on the system, but should be on the order of a few tenths of a volt.

If the network needs readjustment to eliminate the 60 Hz fundamental, set P3 and P4 at midrange. Alternately make small adjustments to P3 and P4 until the desired level is achieved.

Method II - Single Phase Test Source

The basic circuit used in checking the network is shown in Figure 11. This arrangement provides the means of obtaining two test currents of equal magnitude but separated by 60°. Then by appropriate connections to the network it is possible to simulate a balanced negative-sequence current (Table IV). During the following tests the basic current level in each branch will be 5 amps, and since these currents will add at a 60° angle, the total load in the variac will be about 8.7 amps. It is desirable that the 110 volt scale of the phase angle meter be used to minimize the effect of this potential circuit on the relation between the two test currents. It is further desirable that the variac be set near its maximum voltage output and that the load boxes be set to obtain approximately 5 amps as a preliminary step, since this will provide the greatest possible voltage to the phase angle meter and will insure the best possible accuracy.
The negative sequence current is simulated by setting branch "A" current to lag an equal current in branch "B" by 60° and by reversing the branch "B" current at the relay. Branch "A" current now leads the reversed branch "B" current by 120°.

The following procedure is suggested:

1. Make connections per Figure 11 and Table IV.
2. Adjust the branch "B" load box to obtain approximately 5 amps when the Variac is set for 110 volts.
3. Adjust the branch "A" load box until the phase angle meter indicates a 60° lag of current with respect to voltage.
4. Readjust the branch "B" load box until branch "A" and "B" currents are equal.
5. Adjust the Variac until both currents are 5 amps.
6. Touch up branch "A" load box for angle trimming and branch "B" load box for magnitude trimming.

**TABLE IV**

<table>
<thead>
<tr>
<th>TEST FIGURE POINT</th>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLYP51A TERMINAL</td>
<td>YB1</td>
<td>YB7</td>
<td>YB3, YB5</td>
</tr>
</tbody>
</table>

The voltage at the 11Z jack may be a distorted wave at system frequency. With perfectly balanced currents and a network which has been perfectly adjusted, the waveform observed at the 11Z test jack should consist solely of harmonics (primarily third and fifth).

Since perfection is seldom realized, the branch "A" and branch "B" load boxes should now be touched up until the waveform contains no fundamental component, and then the variac readjusted until the branch "B" current is again 5 amps. Branch "A" current should be 5 amps ± 0.5 amps, and the angle between the "A" and "B" currents should be 60° ± 30°. The peak-to-peak value of the network output, which now will consist solely of harmonics, will depend on the system, but should be on the order of a few tenths of a volt.

If the network needs readjustment to eliminate the 60 Hz fundamental, follow steps 1 through 6 above. Set P3 and P4 at mid-range. Alternately make small adjustments to P3 and P4 until the desired level is achieved.

**B. 11Z Magnitude Adjustment And Relay Angle Of Maximum Reach Adjustment**

Since there is some interdependence between these two adjustments, if either one is changed the other should be checked.

**Method I - Three Phase Test Current Source**

Use the test circuit of Figure 12 and the connections of Table V. Set voltage restraint taps at 100%.

**TABLE V**

<table>
<thead>
<tr>
<th>TEST FIGURE POINT</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLYP51A TERMINAL</td>
<td>YA2</td>
<td>YA3</td>
<td>YA4</td>
<td>YB5</td>
<td>YB7</td>
<td>YB1</td>
<td>YB3</td>
</tr>
</tbody>
</table>

Jumper H to I and J to K

It is the nature of this test circuit that the relay angle of maximum reach leads the apparent (measured) angle, by 30°. Thus if an angle of maximum reach of 85° is desired, the apparent (measured) angle will be 55°.
The test procedure is outlined below:

1. Set \( V_{\theta-\phi} \) equal to 26 \( V_{RMS} \) and the current equal to 5 amperes (each phase).

   For testing at restraint taps other than 100%, the phase to phase voltage should equal:

   \[
   V_{\theta-\phi} = \frac{26 \, V_{RMS}}{\% \, RERAINT} \times 100
   \]

2. Adjust phase shifter to obtain desired angle reading on the phase angle meter (30° lagging desired angle of maximum reach).

3. Adjust P6 until the voltage at the \( I_{1\mathcal{Z}} \) test jack is exactly in phase with the voltage at the \( V_1 \) test jack.

4. Adjust P5 until the voltage (RMS) at the \( I_{1\mathcal{Z}} \) test jack exactly equals that at the \( V_1 \) test jack.

5. Repeat steps 3 and 4, if necessary.

**Method II - Single Phase Test Current Source**

Use the test circuit of Figure 13 and the connections of Table VI. These connections simulate a B-C fault.

**TABLE VI**

<table>
<thead>
<tr>
<th>TEST FIGURE POINT</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLYP51A TERMINAL</td>
<td>YA2</td>
<td>YA3</td>
<td>YA4</td>
<td>YA5</td>
<td>YA7</td>
<td>YA3</td>
<td>YA1</td>
</tr>
</tbody>
</table>

It is the nature of this test circuit that the relay angle of maximum reach lags the measured, or apparent line angle by 120°. Thus if an angle of maximum reach of 85° is desired, the apparent angle will be 205°.

The test procedure is outlined below:

1. Set \( V_{\theta-\phi} \) equal to 15 \( V_{RMS} \) (26/\( \sqrt{3} \))", and the current equal to 5 (each phase).

2. Adjust phase shifter to obtain desired angle reading on the phase angle meter (apparent angle of maximum reach leads actual angle of maximum reach by 120°).

3. Adjust P6 until the voltage at the \( I_{1\mathcal{Z}} \) test jack is exactly in phase with the voltage at the \( V_1 \) test jack.

4. Adjust P5 until the voltage (RMS) at the \( I_{1\mathcal{Z}} \) test jack exactly equals that at the \( V_1 \) test jack.

5. Repeat steps 3 and 4 if necessary.

**3Io Circuit Check**

Apply five amperes to the relay per the test circuit of Figure 14 and the connections of Table VII. Check that the voltage (RMS) at the \( I_{1\mathcal{Z}} \) test jack is one third of that obtained by Method I or \( 1/\sqrt{3} \) times that obtained by Method II.

**TABLE VII**

<table>
<thead>
<tr>
<th>TEST FIGURE POINT</th>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLYP51A TERMINAL</td>
<td>YB8</td>
<td>YB10</td>
</tr>
</tbody>
</table>
C. Voltage Restraint Tap Setting

The arrangement of the voltage restraint tap blocks is described under CONSTRUCTION, and the choice of tap settings is discussed in the section on CALCULATION OF SETTINGS. The pickup voltage at the relay angle of maximum reach is given by the relationship.

\[ V_1 = \frac{I_1 \times T_B \times 100}{T} \]

where: \( T \) = Voltage restraint tap setting in percent
\( T_B \) = Basic minimum ohm tap setting
\( I_1 \) = Positive sequence test current

D. Basic Minimum Ohmic Tap Setting

The arrangement of the basic ohmic taps is described under CONSTRUCTION, and the choice of tap settings is discussed in the section on CALCULATION OF SETTINGS. The reach at the relay angle of maximum reach is given by the relationship:

\[ Z_{MAX} = \frac{T_B \times 100}{T} \]

where: \( T \) = Voltage restraint tap setting in percent
\( T_B \) = Basic minimum ohmic tap setting

E. Mho Characteristic Tests
Timer Adjustments And Tests

The pickup setting of the characteristic timer determines the shape of the mho characteristic. Increasing the timer pickup setting tends to narrow the characteristic; decreasing the setting widens the characteristic. The reset time delay (drop out time) of the timer provides an overlap of the next half cycle measurement and produces a continuous logic signal. The timer settings are discussed in the section CALCULATION OF SETTINGS.

Method I - Switched D.C. Input

In order to test the timer cards by this method, it is necessary to remove the card previous to the timer and to place the timer card in a card adapter. The timer test circuit is shown in Figure 15. Opening the N.C. contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer (on the T101 and T107 cards adjust P2) on the timer card clockwise. Closing the contact causes the timer output to drop out after the reset delay setting of the card. To increase the reset time, turn the lower potentiometer (on the T101 and T107 cards adjust P3) on the card clockwise.

The shorter pickup time of the T107 card can be observed at pin 7 on the card. The longer pickup time is factory adjusted by P1 for a pickup 1.2 ms longer than the shorter time. This output must be observed at pin 8.

Method II - AC Inputs

Either the three phase test current source circuit or the single phase test current source circuit shown in section B can be used to provide AC input quantities to adjust the timers.

The test procedure is outlined below:

1) Set the current equal to five amperes.

2) Adjust the voltage until blocks of the desired pick up width are present at the input to the timer card.

3) Turn the dropout potentiometer counter clockwise to decrease dropout time. This allows the pickup time to be observed.

4) Adjust the pickup potentiometer so that the timer just picks up.
5) Turn the dropout potentiometer clockwise until the output is continuous. At this point one additional turn should be given to the potentiometer.

For dropout times greater than 1/4 cycle (MO8, Mj8), the switch DC input method described above must be used. The switches DC input method must also be used to check the longer pickup setting of T107 timer card.

F. Filter Card Phase Shift Adjustment

Each filter card is equipped with an adjustable phase shift in the polarizing circuit. The setting of the polarizing quantity with respect to the operating quantity is discussed in the section CALCULATION OF SETTINGS. The effects of leading and lagging polarizing quantities are shown in Figure 16.

A 4.17 ms characteristic (circle) remains circular if the polarizing voltage is shifted leading or lagging. The area of the circle, however, increases.

To set the polarizing phase shift, use the test circuit of Figure 9 and the connections of Table VIII.

TABLE VIII

<table>
<thead>
<tr>
<th>TEST FIGURE POINT</th>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLYP51A TERMINAL</td>
<td>YA2</td>
<td>YA3</td>
<td>YA4</td>
</tr>
</tbody>
</table>

With 0° polarizing phase shift the outputs at pins 8 and 9 are in phase. Turning P71 counter clockwise causes the polarizing voltage at pin 9 to lag the operate voltage at pin 8; turning P71 clockwise causes the polarizing voltage to lead the operate voltage.

6. V1 Level Detector Adjustment

The positive sequence voltage pickup level setting is discussed in the section CHOICE AND CALCULATION OF SETTING. Using the test circuit of Figure 9 and the connections of Table VIII apply the desired voltage to the relay. Adjust potentiometer P1 until the card just picks up. Turning P1 clockwise increases the pickup level.

PERIODIC CHECKS AND ROUTINE MAINTENANCE

Periodic Tests

All functions included in the SLYP51A relay may be checked at periodic intervals using the procedures described in the section INSTALLATION TESTS. Cable connections between the SLYP51A and the associated Type SLA relay may be checked by observing the test points in the SLA unit.

The following checks should be made during periodic testing:

1. Relay angle of maximum reach setting.
2. Voltage restraint tap setting.
3. Basic minimum ohmic tap setting.
4. Mho characteristic timer setting.
5. Mho characteristic phase angle setting.
6. V1 level detector pickup setting.

Trouble Shooting

In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.
A dual-trace oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

Spare Parts

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The wiring diagrams for the cards in the SLYPS1A relay are included in the card book GEK-34158; the card types are shown on the component location diagram (Figure 2).
FIG. 1 (0227A2036-0) Outline And Mounting Dimensions For The Type SLYPS1A Relay
* SEE INTERNAL 0149C7225 FOR CARDS IN THESE POSITIONS

FIG. 2 (0246A2491-2) Component And Card Locations For The Type SLYP51A Relay

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FIG. 3 (0149C7225-10) Internal Connections For The Type SLYP51A Relay
FIG. 4 (0246Å6887-0) SLYP Positive Sequence Voltage Network
FIG. 5 (0246A6886-0) SLYP Positive Sequence Current Network
FIG. 6 (0246A7984-0) Offset Mho Characteristic By Phase Angle Measurement

(a) EXTERNAL FAULT
B = 90°

(b) BALANCE POINT
B = 90°

(c) INTERNAL FAULT
B < 90°

φ = ANGLE OF MAX. REACH
NOTE: THESE WAVEFORMS ARE SHOWN IN SIMPLIFIED FORM. NORMALLY THE FILTER CARD OUTPUTS ARE PHASE SHIFTED WITH RESPECT TO THE INPUTS.

FIG. 7 (0246A7985-1) SLYP Operating Quantity Waveforms
10% RESTRAINT TAPS

1% RESTRAINT TAPS

MOVABLE LEADS

I₁Z MAGNITUDE POT

TEST JACKS

V₁

I₁Z

P5

I₁Z ADJ

P6

RELAY ANGLE OF MAX REACH ADJ

ANGLE ADJ.

• FIXED TAP
○ ADJUSTABLE TAP

85% VOLTAGE RESTRAINT TAP ILLUSTRATED
REACH = 1.18 T_B

T_B = BASIC MINIMUM OHMIC TAP SETTING

FIG. 8 (0246A6885-1) Typical SLYP Voltage Restraint Tap Settings
TEST SOURCE MUST BE BALANCED

FIG. 9 (0246A6884-1) SLYP Voltage Network Test Connections
TEST SOURCE MUST BE BALANCED

ALL GCX REACTORS MUST BE SET ON THE SAME TAP

\[ \text{\textit{NOTE: REACTOR SHOULD BE ON THE HIGHEST POSSIBLE OHMIC TAP THAT WILL ALLOW THE DESIRED CURRENT TO BE OBTAINED.}} \]

FIG. 10 (0246A6883-1) SLYP Current Network Test Connections-Method I
FIG. 11 (0246A6882-1) SLYP Current Network Test Connections-Method II
TEST SOURCE MUST BE BALANCED

FIG. 12 (0246A6881-1) SLYP Unit Test Circuit-Method I
FIG. 13 (0246A6860-1) SLYP Unit Test Circuit-Method II
FIG. 14 (0246A6879-0) SLYP 310 Test Circuit
FIG. 15 (0246A7987-0) Timer Test Circuit
TIMER SETTING = 2.76ms (60°)

A. $V_{pol} \& V_F$ IN PHASE
   $\alpha_1 = \text{TIMER SETTING} = 60°$
   $\alpha_2 = \text{TIMER SETTING} = 60°$
   $q = 0°$

B. $V_{pol}$ LEADS $V_F$ BY 15°
   $q = 15°$
   $\alpha_1 = \text{TIMER SETTING} + q$
   $= 60° - 15° = 45°$
   $\alpha_2 = \text{TIMER SETTING} - q$
   $= 60° + 15° = 75°$

C. $V_{pol}$ LAGS $V_F$ BY 15°
   $q = -15°$
   $\alpha_1 = 60° - (-15°) = 75°$
   $\alpha_2 = 60° - 15° = 45°$

FIG. 16 (0246A6866-0) Effects Of Polarizing Quantity Phase Shift To Mho Characteristics
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