GE Motors & Industrial Systems

MULTI-BRIDGE SIGNAL PROCESSING BOARD
DS200SPCBG1A_ _

These instructions do not purport to cover all details or variations in equipment, nor to provide every possible contingency to be met during installation, operation, and maintenance. If further information is desired or if particular problems arise that are not covered sufficiently for the purchaser's purpose, the matter should be referred to GE Motors & Industrial Systems.

CONTENTS

SAFETY SYMBOL LEGEND

WARNING — Indicates a procedure, practice, condition, or statement that, if not strictly observed, could result in personal injury or death.

CAUTION — Indicates a procedure, practice, condition, or statement that, if not strictly observed, could result in damage to or destruction of equipment.

NOTE Indicates an essential or important procedure, practice, condition, or statement.

FUNCTIONAL DESCRIPTION

The DS200SPCB Multi-Bridge Signal Processing Board (SPCB) provides an interface between the drive control board and the multi-bridge hub communications board. The SPCB board consists of two encoder follower circuits, two process control analog signal interface circuits, and fiber-optic interface circuits.

The SPCB board performs the following functions:

- Processing encoder feedback signals to the drive control board
- Converting the two analog process control voltage/current signals to ±5 V voltage signals and transmitting the resulting voltage signals to the drive control board
- Providing fiber-optic transmit and receive capabilities for bridge-to-bridge communications and a fiber-optic mode transmission channel for master-to-master systems
- Transmitting and receiving synchronization signals, either through an isolated drive local area network (DLAN) hardware architecture or through fiber-optic sync input and output channels

APPLICATION DATA

ENCODER FOLLOWER CIRCUITS

The two encoder follower circuits include a 3-channel opto-coupled differential interface for channel A, channel B, and marker pulse inputs from an incremental encoder or digital tachometer. The input signals are decoded by PAL (programmable array logic) circuits to produce up/down and marker pulse output signals. These output signals are fed to the drive control board via connector 7PL. The PAL inputs may be 5 V or 15 V differential signals.

PROCESS CONTROL SIGNAL INPUTS

The analog process control input channels SP1 and SP2 are operational amplifier gain circuits. They convert 1 – 5 mA, 4 – 20 mA, 10 – 50 mA, or 2 – 30 V process control input signals into the –5 to +5 V signals that are fed to the drive control board.

ADJUSTABLE HARDWARE

The SPCB board includes Berg-type (manually moveable) jumpers, identified by a JP nomenclature; a DIP switch, designated SW1; and six pots, P1 through P6.
The jumpers are used for manufacturing test or customer options. Most of the jumper selections have been set at the factory. The test data sheets supplied with each controller (typically located in the drive door pocket) indicate these positions. See Table 1 for jumper settings and descriptions.

The switch settings, and their effect on the board's configuration, are shown in Table 2.

The potentiometers (pots) may be adjusted during startup to optimize drive performance. The initial setting is the straight-up (12 o'clock) position (see Figure 1). (The limit of rotation is approximately 150 degrees in either direction from the straight-up position.) See Table 3 for a listing of the SPCB board's pots, pot descriptions, and default positions.

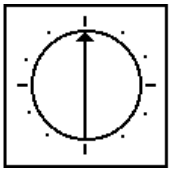

Figure 1. Pot Set At Straight-Up Position

NOTE

When replacing an SPCB board, make sure that the jumpers and switches on a replacement board are placed the same as on the old board, unless the instructions indicate otherwise. Set each pot approximately the same as on the old board. (Figure 2 shows the locations of the SPCB board's jumpers, DIP switch, and pots.)

INPUT/OUTPUT (I/O)

The location of each I/O connector is shown on Figure 2. Encoder and channel inputs are received simultaneously through ribbon cable connector **16PL** and terminal block **1TB**. See Table 4 for the nomenclatures and descriptions of each pin/terminal.

Connector **SYTB** outputs the drive synchronization signals to the drive control board. See Table 5 for the nomenclatures and descriptions of each pin.

Ribbon cable connector **7PL** supports I/O between the SPCB board and the drive control board. See Table 6 for the nomenclatures and descriptions of each pin / terminal.

The SPCB board includes blue fiber-optic receivers and gray fiber-optic transmitters. Bridge-to-bridge communications (COMM) are supported by the fiber-optic devices at positions U11 and U20. The fiber-optic devices at U27 and U26 (SYNCH) provide an alternate channel for drive synchronization. The fiber-optic transmitter at U28 (MODE) is used when this drive is part of a master-to-master system. See Table 7 for the nomenclatures and descriptions of each fiber-optic device.

TESTPOINTS

Testpoints and signal nomenclatures are listed in Table 8. See Figure 2 for the location of each testpoint.

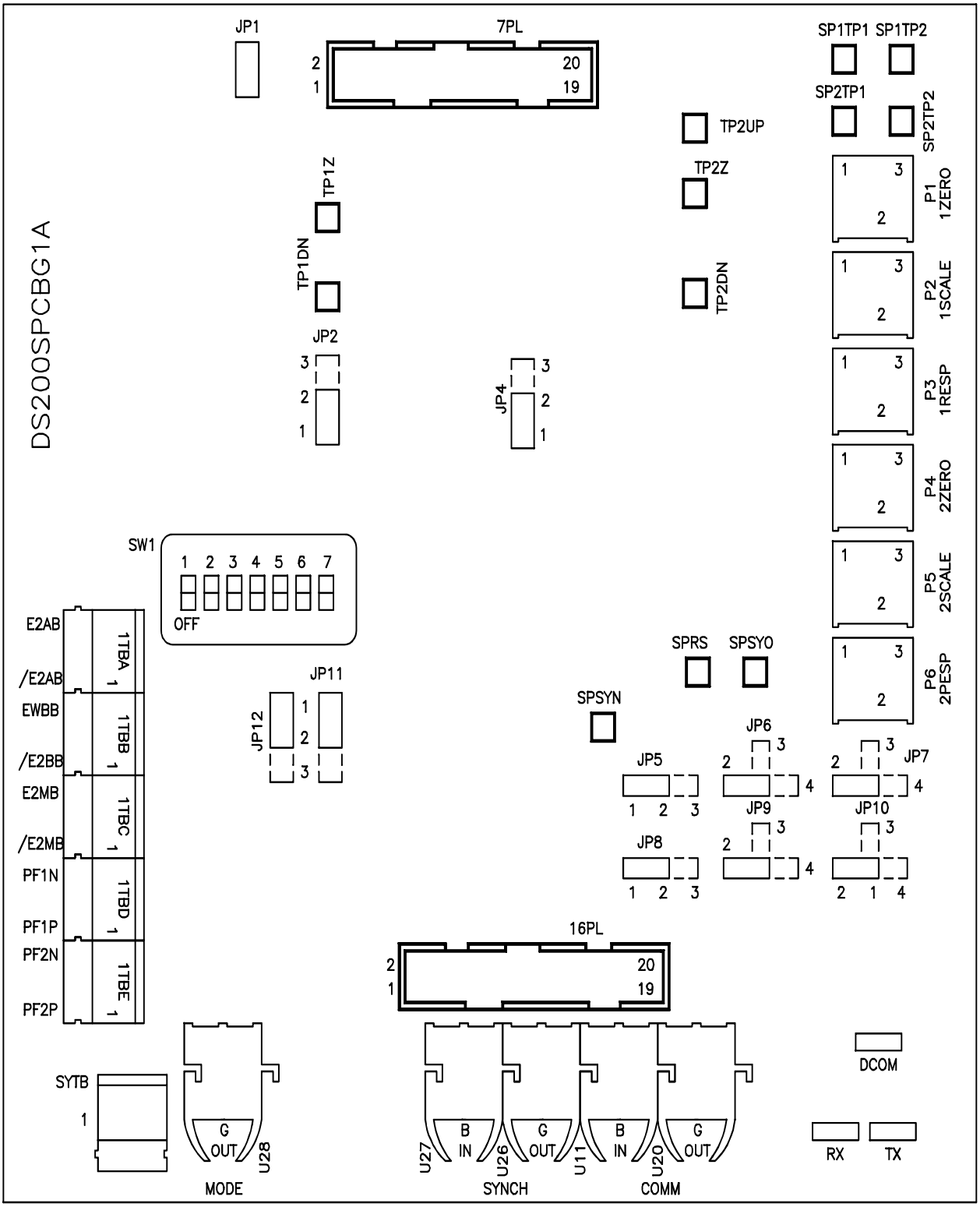

Figure 2. SPCB Board Layout Diagram

Table 1. Jumpers

Name	Description
JP1	Encoder #1 and #2 clock inhibit, this is used for test purposes only. 1.2 Enables encoder logic array (normal operation) 0 Inhibits clock to PAL (manufacturing test only)
JP2	Encoder #1 marker channel enable to be used for absolute position. 1.2 Inhibit marker, for incremental position or speed only 2.3 Enable marker, for absolute position instrumentation
JP4	Encoder #2 marker channel enable to be used for absolute position. 1.2 Inhibit marker, for incremental position or speed only 2.3 Enable marker, for absolute position instrumentation
JP5	Select gain of amplifier for the analog channel SPA1 (VAR.256) Jumpers JP5 - JP7 and pots P1 - P3 on the SPCB board control hardware options for the process follower analog channel SPA1 (VAR.256), input from PF1P and PF1N on 1TB. This circuit is a general purpose amplifier which can accept either current loop or voltage inputs. JP7 and P1 (1ZERO) control the offset added to the input; JP5 and P2 (1SCALE) control the gain of the amplifier, CW = more gain; P3 (1RESP) controls the response of the low pass filter of the amplifier, CCW = more filtering; and JP6 controls input burdening when this circuit is used for current loop inputs. The most common configurations are as follows: PF1P/PF1N MODE JP5 JP6 JP7 1-5 mA 1.2 1.3 1.3 4-20 mA 1.2 1.3 1.3 10-50 mA 1.2 1.4 1.3 0-30 V 1.2 1.2 1.3 For example, to set-up a 4-20 mA current loop, assuming PF1P positive with respect to PF1N: - Set JP5 1.2 and JP6 1.3. Temporarily set JP7 to 1.2. - Apply a 20 mA input, and adjust P2 until testpoint SP1TP2 is 6.25 V. - Set JP7 to 1.3. - Adjust P1 until SP1TP2 is 5.0 V and VAR.256 is +500 counts. - Apply a 4 mA input, and verify that SP1TP2 and VAR.256 are both 0. If the ratio between the maximum and minimum inputs is not 5, the voltage at SP1TP2 for the second step should be adjusted to (5 × max)/(max - min) V instead of 6.25 V. Note that VAR.256 saturates at a maximum value of +511 counts when SP1TP2 exceeds 5 V. Also note that currents less than 4 mA produce negative values down to -512 counts at VAR.256. If this is undesirable, feed VAR.256 into a limit block before using it in the drive. 1.2 Normal gain 2.3 10:1 gain boost for max input < 5 mA or < 2 V
JP6	Select input burdening for PF1P/PF1N of the analog channel SPA1 (See JP5) 1.2 No burden, for 2-30 V dc input signals (see JP5) 1.3 Burden for 1-5 or 4-20 mA current loop input 1.4 Burden for 10-50 mA current loop input
JP7	Select zero offset for the analog channel SPA1 (see JP5). Use P1 for fine trim. 1.2 No offset 1.3 Negative offset 1.4 Positive offset

Table 1. Jumpers – Continued

Name	Description
JP8	Select gain of amplifier for the analog channel SPA2 (VAR.257) Jumpers JP8 - JP10 and pots P4 - P6 on the SPCB board control hardware options for the process follower analog channel SPA2 (VAR.257), input from PF2P and PF2N on 1TB. This circuit is a general purpose amplifier which can accept either current loop or voltage inputs. JP10 and P4 (2ZERO) control the offset added to the input; JP8 and P5 (2SCALE) control the gain of the amplifier, CW = more gain; P6 (2RESP) controls the response of the low pass filter of the amplifier, CCW = more filtering; and JP9 controls input burdening when this circuit is used for current loop inputs. The most common configurations are as follows: PF2P/PF2N MODE JP8 JP9 JP10 1-5 mA 1.2 1.3 1.3 4-20 mA 1.2 1.3 1.3 10-50 mA 1.2 1.4 1.3 0-30 V 1.2 1.2 1.3 For example, to set-up a 1-5 mA current loop, assuming PF2P positive with respect to PF2N: - Set JP8 1.2 and JP9 1.3. Temporarily set JP10 to 1.2. - Apply a 5 mA input, and adjust P5 until Test point SP2TP2 is 6.25 V. - Set JP10 to 1.3. - Adjust P4 until SP2TP2 is 5.0 V, and VAR.257 is +500 counts. - Apply a 1 mA input, and verify that SP2TP2 and VAR.257 are both 0. If the ratio between the maximum and minimum inputs is not 5, the voltage at SP2TP2 for the second step should be adjusted to (5 × max)/(max - min) V instead of 6.25 V. Note that VAR.257 saturates at a maximum value of +511 counts when SP2TP2 exceeds 5 V. Also note that currents less than 1 mA produce negative values down to -512 counts at VAR.257. If this is undesirable, feed VAR.257 into a limit block before using it in the drive. 1.2 Normal gain 2.3 10:1 gain boost for max input < 5 mA or < 2 V
JP9	Select input burdening for PF2P/PF2N of the analog channel SPA2 (See JP8) 1.2 No burden, for 2-30 V dc input signals (see JP8) 1.3 Burden for 1-5 or 4-20 mA current loop input 1.4 Burden for 10-50 mA current loop input
JP10	Select zero offset for the analog channel SPA2 (see JP8). Use P4 for fine trim. 1.2 No offset 1.3 Negative offset 1.4 Positive offset
JP11	Jumper selects whether to listen to the fiber-optic or hardware (hard-wired) channel for the synchronization signal. 1.2 Listen to hardware sync channel 2.3 Listen to fiber-optic sync channel
JP12	Enable or disable master sync signal derived from drive control board. Setting 1.2 is for follower bridges. 1.2 restricts the bridge to be a "listener." If drive is a master this jumper must be 2.3. Setting 2.3 allows the synchronization signal to be transmitted on the fiber-optic channel or the hardware (hard-wired) sync channel. 1.2 Disable master sync input (Drive is a multi-bridge FOLLOWER) 2.3 Enable master sync input (Drive is a MASTER)

Table 2. Switches

Name	Description
SW1-1	Selects input attenuation resistors for channel A of encoder #1 Input attenuation resistors for channel A of encoder #1 can be selected as follows: 0 (Off) 15 V encoder interface 1 (On) 5 V encoder interface
SW1-2	Selects input attenuation resistors for channel B of encoder #1 Input attenuation resistors for channel B of encoder #1 can be selected as follows: 0 (Off) 15 V encoder interface 1 (On) 5 V encoder interface
SW1-3	Selects input attenuation resistors for marker channel of encoder #1 Input attenuation resistors for marker channel of encoder #1 can be selected as follows: 0 (Off) 15 V encoder interface 1 (On) 5 V encoder interface
SW1-4	Selects input attenuation resistors for channel A of encoder #2 Input attenuation resistors for channel A of encoder #2 can be selected as follows: 0 (Off) 15 V encoder interface 1 (On) 5 V encoder interface
SW1-5	Selects input attenuation resistors for channel B of encoder #2 Input attenuation resistors for channel B of encoder #2 can be selected as follows: 0 (Off) 15 V encoder interface 1 (On) 5 V encoder interface
SW1-6	Selects input attenuation resistors for marker channel of encoder #2 Input attenuation resistors for marker channel of encoder #2 can be selected as follows: 0 (Off) 15 V encoder interface 1 (On) 5 V encoder interface
SW1-7	Spare switch, not used

Table 3. Pots and Descriptions

Pot	Nomenclature	Description
P1	1ZERO	Provides zero adjust of SPA1 (see Table 1, JP5) Default position straight-up
P2	1SCALE	Provides gain adjust of SPA1 (see Table 1, JP5) Default position fully counterclockwise
P3	1RESP	Adjusts the response of analog channel #1 (SPA1) - The response can be adjusted from 1 to 1000 msec. Default position fully counterclockwise
P4	2ZERO	Provides zero adjust of SPA2 (see Table 1, JP8) Default position straight-up
P5	2SCALE	Provides gain adjust of SPA2 (see Table 1, JP8) Default position fully counterclockwise
P6	2RESP	Adjusts the response of analog channel #2 (SPA2) - The response can be adjusted from 1 to 1000 msec. Default position fully counterclockwise

Table 4. Inputs from External Connections 16PL and 1TB

16PL Pin No.	1TB Terminal	Nomenclature	Description
1	------	E1AB	Non-inverting input for encoder #1 channel A
2	------	/E1AB	Inverting input for encoder #1 channel A
3	------	E1BB	Non-inverting input for encoder #1 channel B
4	------	/E1BB	Inverting input for encoder #1 channel B
5	------	E1MB	Non-inverting input for encoder #1 marker channel
6	------	/E1MB	Inverting input for encoder #1 marker channel
7	1	E2AB	Non-inverting input for encoder #2 channel A
8	2	/E2AB	Inverting input for encoder #2 channel A
9	3	E2BB	Non-inverting input for encoder #2 channel B
10	4	/E2BB	Inverting input for encoder #2 channel B
11	5	E2MB	Non-inverting input for encoder #2 marker channel
12	6	/E2MB	Inverting input for encoder #2 marker channel
13	7	PF1N	Inverting input for analog channel SPA1 (VAR.256)
14	8	PF1P	Non-inverting input for analog channel SPA1 (VAR.256)
15	9	PF2N	Inverting input for analog channel SPA2 (VAR.257)
16	10	PF2P	Non-inverting input for analog channel SPA2 (VAR.257)
17	11	TXP	Not Connected
18	12	TXN	Not Connected
19	13	RXN	Not Connected
20	14	RXP	Not Connected

Table 5. Connector SYTB, Drive Synchronization Output

Pin No.	Nomenclature	Description
1	SYNC	Drive synchronization signal, non-inverting
2	/SYNC	Drive synchronization signal, inverting

Table 6. Connector 7PL, I/O Between SPCB Board and Drive Control Board

Pin No.	Nomenclature	Direction	Description
1	SPA1	Output	±5 V dc SPCB analog channel #1
2	SPA2	Output	±5 V dc SPCB analog channel #2
3	E1Z	Output	Marker channel from encoder #1 interface
4	E2Z	Output	Marker channel from encoder #2 interface
5	N15	Output	Negative 15 V dc power supply for analog circuitry
6	P15	Output	Positive 15 V dc power supply for analog circuitry
7	DCOM	Output	Power supply return
8	SPRS	Input	Digital input
9	DCOM	Output	Power supply return, common
10	P5	Output	Positive 5 V dc power supply for digital circuitry

Table 6. Connector 7PL, I/O Between SPCB Board and Drive Control Board – Continued

Pin No.	Nomenclature	Direction	Description
11	E1UP	Output	Up channel output from encoder #1 interface
12	E1DN	Output	Down channel output from encoder #1 interface
13	E2UP	Output	Up channel output from encoder #2 interface
14	E2DN	Output	Down channel output from encoder #2 interface
15	0RST7	N/A	Not Connected
16	DCOM	Output	Power supply return, common
17	SPSYN	Output	Sync pulse listener input to drive control board
18	SPSYO	Input	Sync pulse output from drive control board
19	SPTX	Input	+5 V dc input from drive control board's Motor Control Processor (MCP) UART
20	SPRX	Output	+5 V dc output to MCP UART

Table 7. FIber-optic Connectors

Location	Nomenclature	Color	Description
U11	COMM	Blue	Bridge-to-bridge communications (COMM IN/COMM OUT) occur through this channel through the MBHA board. It should connect to one of the following channels on the MBHA board, depending on which drop the respective bridge is: Control1, Control2, Control3, Control4, or Control5. Blue is the receiver, gray is the transmitter.
U20	COMM	Gray	
U26	SYNCH	Gray	Bridge-to-bridge firing synchronization occur through this channel through the MBHA board. If it is used, it should connect to one of the following channels on the MBHA board, depending on which drop the respective bridge is: Control1, Control2, Control3, Control4, or Control5. Blue is the receiver, gray is the transmitter.
U27	SYNCH	Blue	
U28	MODE	Gray	Transmission channel to support master-to-master configuration.

Table 8. Testpoints

Testpoint	Revision	Description
TP1UP	All	Encoder #1 up counter output - During forward encoder rotation, TPnUP will have a narrow pulse at the edges of each encoder tooth.
TP1DN	All	Encoder #1 down counter output - During reverse encoder rotation, TPnDN will have a narrow pulse at the edges of each encoder tooth.
TP1Z	All	Encoder #1 marker channel output (if enabled) - If enabled, a narrow pulse will occur coincident with the leading edge of the marker pulse.
TP2UP	All	Encoder #2 up counter output
TP2DN	All	Encoder #2 down counter output
TP2Z	All	Encoder #2 marker channel output (if enabled)
RX	All	Fiber-optic communications receiver input to drive control board, Fiber-optic bridge receiver (COMM IN) testpoint
TX	All	Fiber-optic communications transmitter output from drive control board, Fiber-optic bridge transmitter (COMM OUT) testpoint
SP1TP1	All	SPA1 differential amplifier output, ahead of potentiometer P1/P2 offset and scaling
SP1TP2	All	Final output of SPA1 analog input channel, analog version of VAR.256 - An analog voltage of ±5 V dc converts to ±511 counts at VAR.256.
SP2TP1	All	SPA2 differential amplifier output, ahead of potentiometer P4/P5 offset and scaling
SP2TP2	All	Final output of SPA2 analog input channel, analog version of VAR.257 - An analog voltage of ±5 V dc converts to ±511 counts at VAR.257.
SPSYO	All	Sync pulse output from drive control board - This testpoint normally contains the sync pulse output of this particular drive, regardless of whether it is selected as the master sync to all drives of a multi-bridge configuration.
SPSYN	All	Sync pulse listener input to drive control board - In a multi-bridge configuration, this signal is the common ac line sync passed to all drives if the signal is being derived from the hardware (hardwired) or fiber-optic (SYNC IN/SYNC OUT) sync.
SPRS	All	Select local/broadcast mode or used for voting, general purpose signal from the drive control board - In multi-bridge master drives, it is used to select local or broadcast mode for the LAN fiber-optic hub card (MBHA). In multi-bridge follower drives, SPRS may be used for voting on masters for redundant operation.
DCOM	All	Testpoint at signal level common

RENEWAL/WARRANTY REPLACEMENT

BOARD IDENTIFICATION

A printed wiring board is identified by an alphanumeric part (catalog) number stamped on its edge. For example, the SPCB board is identified by part number DS200SPCBG#rrr.

Figure 3 describes each digit in the part number.

NOTE

All digits are important when ordering or replacing any board.

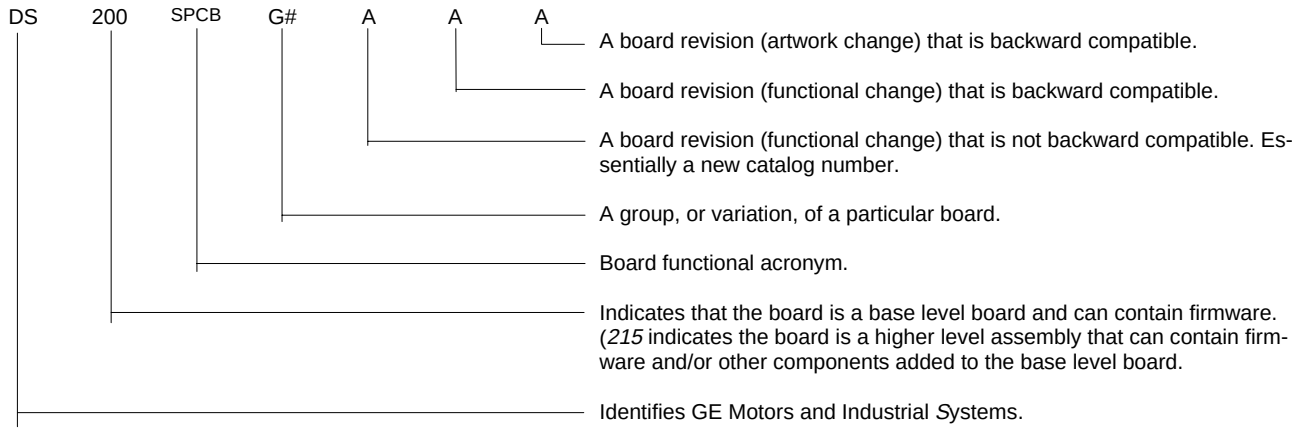

Figure 3. Sample Board Part Number, DS Series

WARRANTY TERMS

The *GE Motors & Industrial Systems Terms and Conditions* brochure details product warranty information, including the **warranty period** and **parts and service** coverage.

The brochure is included with customer documentation. It may also be obtained separately from the nearest GE Sales Office or authorized GE Sales Representative.

WARRANTY PARTS AND SERVICE

This board has no fuses or other end-user serviceable parts. If it fails, it needs to be replaced as a unit. To obtain a replacement board, or service assistance, contact the nearest GE Service Office. Please have the following information ready to exactly identify the **part** and **application**:

- GE requisition or shop order number
- Equipment serial number and model number
- Board number and description

PROCEDURE FOR REPLACING BOARDS

WARNING

To prevent electric shock, turn off power to the board, then test to verify that no power exists in the board before touching it or any connected circuits.

CAUTION

To prevent equipment damage, do not remove boards or connections, or re-insert them, while power is applied to the drive. Treat all boards as static-sensitive. Use a grounding strap when changing boards and always store boards in anti-static bags or boxes they were shipped in.

To replace an SPCB board:

1. **Turn off power to the drive**, then wait several minutes for all capacitors to discharge. Test any electrical circuits before touching them to make sure power is off.

2. Open the drive's cabinet door to access the printed wiring boards.

   - The SPCB board is mounted on the drive control board located in the front position of the front carrier in the board rack.

3. Disconnect all cables from the SPCB board as follows: (Ensure that all cables and wires are labeled to simplify reconnection.)
   - For ribbon cables, grasp each side of the cable connector that mates with the board connector and gently pull the cable connector free.
   - For cables with pull tabs, carefully pull the tab.
   - For wires attached to connectors 1TB and SYTB, loosen the screw located at the top of each terminal and gently pull each wire free.
   - For fiber-optic connectors, depress the latch on the mating cable connector.
4. Remove the four screws with nylon washers that secure the SCPB board to the standoffs on the drive control board, then remove the SPCB board.

CAUTION

Avoid dropping the hardware into the unit, which could cause damage.

NOTE

Because of upgrades, boards of different revision levels may not contain identical hardware. However, GE Motors & Industrial Systems ensures backward compatibility of replacement boards.

5. Set all configurable items on the replacement (new) board in the exact position as those on the board being replaced (old board). Set all pots in the approximate positions of those on the board being replaced.
   - If a board revision has added or eliminated a configurable component, or re-adjustment is needed, refer to Tables 1 – 3.
6. Orient the new SPCB board in the same position as the board removed and mount it on the four standoffs with the four screws with nylon washers removed in step 4. (Make sure that all screws are securely tightened.)
7. Reconnect all cable connectors that were disconnected in step 3. Make sure that connectors are properly seated at both ends.
8. Reconnect all individual wires that were disconnected in step 3. Make sure that each wire is properly secured in the terminal.
9. Reconnect all fiber-optic connectors (if used) that were disconnected in step 3. Make sure that the fiber-optic cable connector latch is engaged to secure the fiber-optic cable.

Notes:

GE Motors & Industrial Systems

Issue Date, Rev. A: May 1997

General Electric Company
Industrial Systems
1501 Roanoke Blvd.
Salem, VA 24153-6492 USA